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4. Document Revision History

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5. Introduction

This specification defines

a. the clocking of the STS-192 / STM-64 SERDES and SONET/SDH framer,

b. the interface at the STS-192 / STM-64 SERDES, connecting to the SONET/SDH framer ASIC

This specification does not define other control/status signals that may be implemented in a module containing the serdes and optical transceivers.

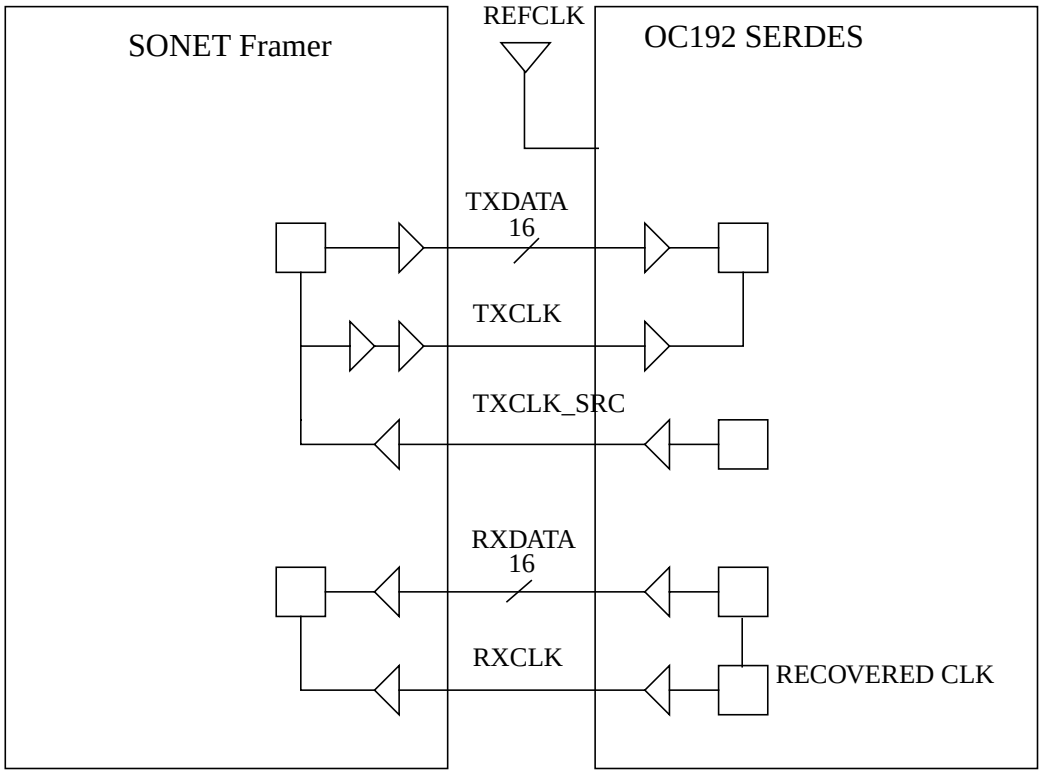
An aggregate of 9953.28 Mb/s is transferred in each direction. Sixteen 622.08 Mb/s differential data lines are provided in the transmit direction, and another sixteen in the receive direction.

This specification is independent of the type of optics which are used.

Because this specification applies to both SONET and SDH, the term OC-192 should be interpreted as applying to both STS-192 and STM-64. This specification applies to speeds up to 10.66 Gb/s.

The diagram below shows the direction of the interface signals. The framer and the SERDES need not be implemented as a single chip each.

Figure 5-1: Diagram of Interface.



6. Interface Description Summary

Table 6-1: Interface Description for the OC192 SERDES.

PIN NAME	I/O TYPE w.r.t. SERDES	DESCRIPTION
TXDATA[15:0]_P/N[1]	input, diff. LVDS	622.08 Mb/s per pin, transfers 16 bits of data from the SONET framer ASIC to the MUX device.
TXCLK_P/N[2]	input, diff. LVDS	622.08 MHz/311 MHz, source synchronous clock for TXDATA. Frequency is mode selectable.
TXCLK_SRC_P/N	output, diff. LVDS	622.08 MHz, Reference clock from the SERDES to the SONET framer ASIC.
RXDATA[15:0]_P/N[1]	output, diff. LVDS	622.08 Mb/s per pin, Received data from the DEMUX to the SONET framer ASIC.
RXCLK_P/N	output, diff. LVDS	622.08 MHz, Received clock to qualify RXDATA. Maximum frequency is +2500ppm relative to REFCLK which is a minimum period of 1604 picoseconds.
REFCLK_P/N	input, diff. LV-PECL[4]	622.08 MHz, Board level reference provided.
PHASE_INIT[3]	input, LV-TTL	Optional. Asynchronous, low speed signal. Resets the SERDES clocking interface. Minimum active high pulse width is 5 microseconds.
PHASE_ERR[3]	output, LV-TTL	Optional. Low speed signal. Indicates that the phase of the TXCLK wrt the internal SERDES clock is out of spec.
SYNC_ERR	output, LV-TTL	low speed signal. Indicates RXCLK and RXDATA are not derived from the optical receive signal

1. For OC-192, bit 15 is the MSB and bit 0 is the LSB. The MSB is transferred first.
2. "_P" signals have the true logic level associated with them. "_N" signals are the complements (negated).
3. required if a delay-locked loop method is used for handling forward clocking
4. On the SERDES, at the input of REFCLK_P/N, LVPECL voltage levels are required with external termination, allowing AC or DC connection.

7. Clocking Architecture

7.1 SERDES Vendor Requirements

7.1.1 Transmitter Clocking Functions

1. The transmitter shall provide a clock multiplier PLL to generate the 9.95328 GHz transmit bit rate from a 622.08 MHz LV-PECL reference clock input (REFCLK). Other reference clock frequencies in addition to 622.08 MHz are allowed by this interface standard and are considered optional and vendor specific.
2. The clock multiplier performance shall be guaranteed within the duty cycle of the reference clock specified in table 9-4.
3. Jitter on the optical transmit signal shall comply with the latest Telcordia GR-1377 spec. (Once ITU-T G.783 proposal becomes a standard, the authors of this spec need to review it and apply the ITU jitter requirements as deemed appropriate.)
    a. The reference clock input must meet the jitter specifications up to a jitter frequency of 10 MHz.
    b. The SERDES PLL must meet the jitter specifications at jitter frequencies above 1 MHz.
4. The clock multiplier shall provide an indication if lock to the reference is not achieved or if either the REFCLK or VCO feedback clock signal are not active.
5. It is desirable that the PLL provide an LVPECL clock output (PLLOUT622) at the same rate as the reference clock input (REFCLK). This allows monitoring of the PLL output for test purposes, such as measuring generated jitter, at 622MHz.
6. The transmitter shall preferably provide means to absorb the delay variance between the Framer TXCLK_SRC input and the TXCLK output.
7. If a "Delay Locked Loop" is used to emulate source synchronous clocking then:
    a. A PHASE_INIT input signal shall be provided to indicate when the phase relationship of clock and data is stable and can be locked in, allowing for the greatest tolerance to phase shift during operation (< T/2 or greater with a FIFO).
    b. A “PHASE_ERR” output signal shall be provided to indicate if the phase relationship between TXDATA and TXCLK drift too close to the internal sampling point or FIFO limits used by the SERDES. This signal shall be of a set and hold type, with clearing upon PHASE_INIT assertion.

7.1.2 Optical Receiver Clocking Functions

1. Optical receiver lock range shall exceed +/- 100ppm over temperature and voltage range.
2. Jitter tolerance of the optical receiver shall meet or exceed the limits specified in latest Telcordia GR-1377. (Once ITU-T G.825 proposal becomes a standard, the authors of this spec need to review it and apply the ITU jitter requirements as deemed appropriate.)
3. RXCLK is usually derived from the optical receive signal by dividing down the recovered clock, except under conditions 4.) or 5.) below.
4. Under a LOS condition, the output receive clock rate (RXCLK) shall be set by the external 622.08 MHz LVPECL reference (REFCLK).

5. When the clock rate of the optical received signal deviates by more than 1000ppm, the output receive clock (RXCLK) rate shall be set by an external reference (i.e. somewhere between 100 ppm and 1000 ppm, an out of lock condition should be declared and no errors shall occur until an out of lock is indicated).
6. Under conditions 4 or 5 above - i.e. whenever the receive clock output (RXCLK) and data (RXDATA) are not derived from the optical receive signal:
    a. An error indication (SYNC_ERR) shall be provided.
    b. Switching of the receive clock (RXCLK) shall be done such that minimum pulse widths and minimum period of the receive clock (RXCLK) and data (RXDATA) are not violated.

8. Voltage Levels, Topology, and Terminations

All nets are point-point.

All specifications below must be met over temperature, voltage (nominal +/-5%), and process.

Table 8-2: Voltage level summary.

	LVDS STANDARD NAME	DESCRIPTION	VALUE	SAME AS STANDARD
Driver DC spec	Output differential voltage	single-ended output voltage p-p	250-600mV [1]	yes [1]
Receiver DC spec	Input differential threshold	single-ended input voltage p-p	>= 100mV	yes
	Input voltage range		800-2400mV	no [3]
	Receiver differential input impedance - on-chip termination required		80-120 Ohms	no [2]

[1] Output differential voltage - see Vswing, defined in Figure on SERDES Outputs, in the Timing section. Standard requires 250-400mV. This is a subset of the range allowed, since a larger swing is encouraged but not required.
[2] Impedance range - is wider than specified in the LVDS standard to account for fabrication variability common in today's semiconductor technologies.
[3] Input voltage range - only a subset of the LVDS standard specified range (0-2400mV) is allowed to simplify receiver design.

8.1 SERDES and Framer driver spec

Unless otherwise specified, the driver DC specifications of the LVDS General Purpose Link must be satisfied. For the LVDS Standard reference, see IEEE Std 1596.3-1996, p. 8.

Output differential voltage, as defined in the LVDS standard, is measured at the driver output pin.

8.2 SERDES and Framer receiver spec

Unless otherwise specified, the receiver DC specifications of the LVDS General Purpose Link must be satisfied. For the LVDS Standard reference, see IEEE Std 1596.3-1996, p. 8.

"Input differential threshold" is defined across the receiver input pins. Its value is defined by the LVDS standard and repeated in the table above. It must be valid over process, voltage, temperature.

On-chip current-source biasing, as opposed to external biasing through discrete bias resistors, is recommended, but not a requirement. Lack of discrete resistors simplifies board layout. (By not making on-chip biasing a requirement, vendors have a wider choice of I/O technologies, such as an improved LVDS with on-chip biasing or a 2.5V PECL with external biasing.)

In one possible system implementation, the SERDES would reside on a separate module. In this case, the Framer could be driving a powered-down SERDES. To prevent potential damage to the SERDES inputs in this implementation, the following is recommended.

NOTE— It is recommended that the SERDES input circuits can tolerate being driven by the Framer, even when the SERDES is powered down.

9. Timing

Source synchronous timing is used in both directions.

There are no separate jitter specifications. The timing numbers given are assumed to include variations due to jitter.

These parameters are defined at the pins of the SERDES package in the first sections, and at the pins of the Framer package, in the latter sections. Timing variables are defined by the figures below.

The following approach is taken for positioning clocks. For both the Framer and SERDES drivers, clock edges align to data edges, simplifying the driver macro design. For both the Framer and SERDES receivers, clock edges are centered in the data bit, simplifying the receiver macro design. Delaying the clock to center it within the data bit is achieved on the board, e.g. by swapping clock traces or delaying the clock by other means. One exception to this rule is the 311 MHz clock mode from Framer to SERDES. Here, swapping clock traces is not feasible as a delay method, so the 311 MHz clock delay must be implemented on the SERDES.

All specifications below are suggested to be met over temperature, voltage (nominal +/-5%), and process

The Framer delay variance between the TXCLK_SRC input and the TXCLK output needs to be consistent with the delay variance tolerance of the SERDES.

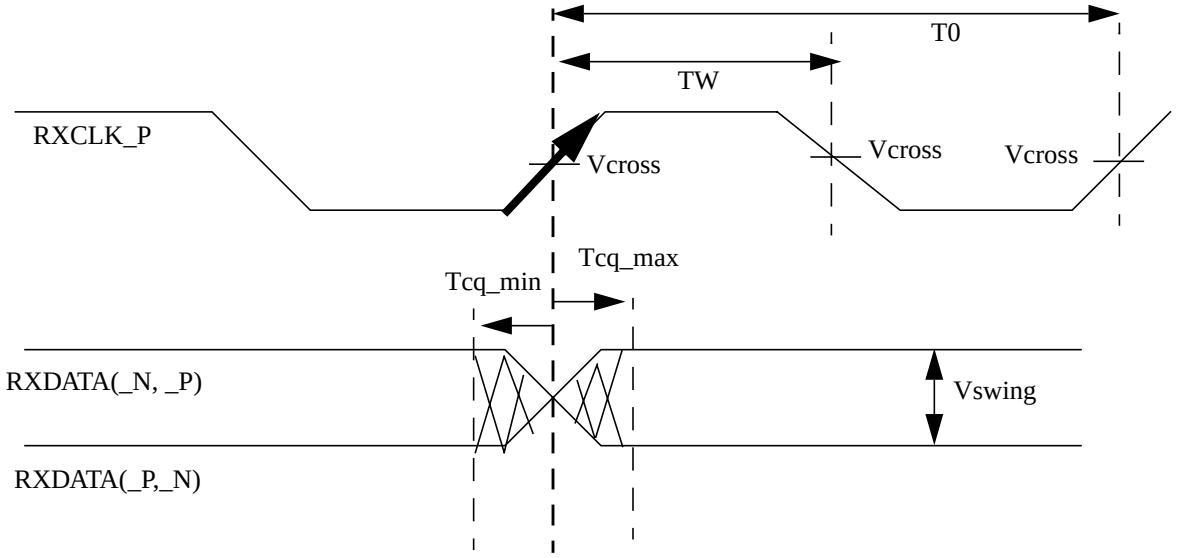
9.1 SERDES outputs

The SERDES LVDS outputs must satisfy the following conditions.

The data received at the SONET framer ASIC must satisfy setup and hold conditions. Working back to the SERDES pin, these conditions are shown in the figure below.

CAUTION—Note that the required data valid window at the SONET framer ASIC are large, leaving only a small timing window for SERDES output skew.

Figure 9-2: SERDES output waveforms at SERDES pin, i.e. receive direction.



RXDATA must satisfy the rise/fall time specifications in the table. RXCLK must meet all the specifications in the table.

TXCLK_SRC will meet the rise/fall time specifications in the table. A tight duty cycle is defined in the table. This is necessary in order for TXCLK, at the output of the Framer, to have acceptable duty cycle as well.

Table 9-3: SERDES Output Timing Parameters.

PARAMETER SYMBOL	DESCRIPTION	VALUE
T0 (see figure)	clock period	1/(622.08 MHz) ~ 1.608ns
TW/T0	duty cycle = high going clk pulse width divided by clk period	0.45 < TW/T0 < 0.55
TR, TF	20-80% rise, fall times	100-250 ps
Tcq_min, Tcq_max (see figure)	clock-output times. defines data invalid window with respect to clock at SERDES pin	200ps , 200ps

9.2 SERDES Inputs, Two Clock Modes

Two clock modes exist.

In the 311 MHz clock mode, the SONET framer ASIC transmits a 311.04 MHz clock along with the data. In the 622 MHz clock mode, the SONET framer ASIC transmits a 622.08 MHz clock along with the data.

The advantage of the 622 MHz clock mode is that a 622 MHz clock seems to be more prevalent in current designs. The advantage of the 311 MHz clock mode is that it is more compatible with today's ASIC technology, since ASIC I/O drivers are typically not well suited for sending 622 MHz signals.

NOTE— It is a REQUIREMENT that the 622 MHz clock mode be supported. It is highly recommended, but not required, that both the 311 and the 622MHz modes be supported, in order to maximize compatibility with other vendors' parts.

9.3 SERDES Inputs, Required 622 MHz Clock Mode

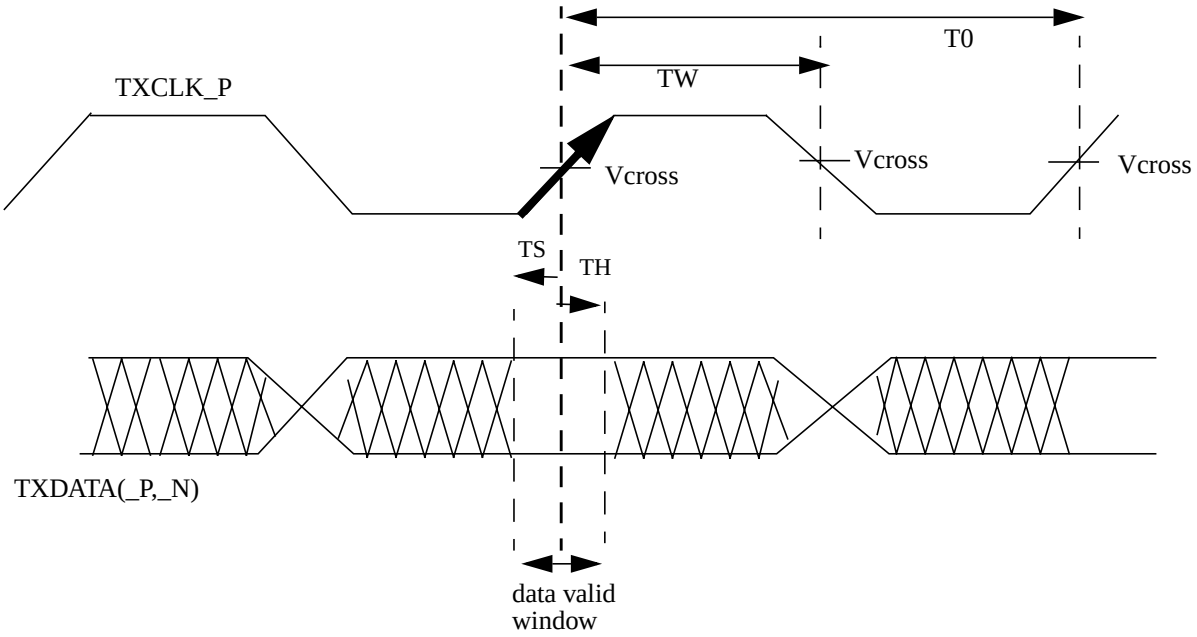
NOTE— In the 622 MHz clock mode, the SONET framer ASIC transmits a 622.08 MHz clock along with the data.

The SERDES LVDS inputs must satisfy the following conditions.

The data is transmitted from the SONET framer ASIC with a given clock-output uncertainty. When observed at the SERDES pin, these conditions are shown in the figure below.

CAUTION—The SERDES must tolerate a large data invalid window generated by the SONET framer ASIC, leaving only a small timing window for SERDES input uncertainty.

Figure 9-3: SERDES input waveforms at SERDES pin, i.e. transmit direction.



TXCLK will meet the duty cycle and rise/fall time specifications in the table. TXDATA will meet the rise/fall time specifications.

REFCLK will meet the rise/fall time and duty cycle specifications in the table 9-4.

Table 9-4: SERDES Input Timing Parameters, for 622 MHz clock mode.

PARAMETER SYMBOL	DESCRIPTION	VALUE
T0 (see figure)	clock period	1/(622.08 MHz)
TW/T0	duty cycle = high going clk pulse width divided by clk period	0.4 < TW/T0 < 0.6
TR, TF	20-80% rise, fall times	100-300 ps [1]
TS, TH	setup time, hold time. defines data valid window with respect to clock at SERDES pin	300 ps, 300 ps

[1] Note that this range assumes a nominal 100 Ohm termination (does not include reflections).

9.4 SERDES Inputs, 311 MHz Clock Mode

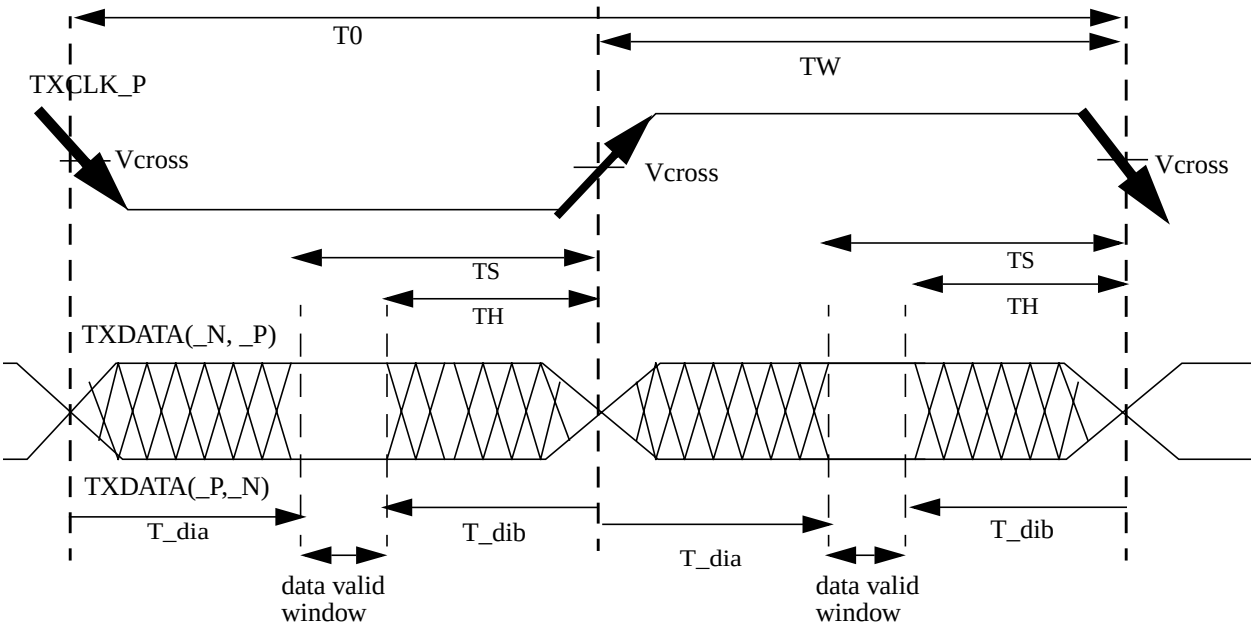
NOTE— In the 311 MHz clock mode, the SONET framer ASIC transmits a 311.04 MHz clock along with the data. The data bits are driven on both edges of the 311 MHz clock.

The SERDES LVDS inputs must satisfy the following conditions.

The data is transmitted from the SONET framer ASIC with a given clock-output uncertainty. When observed at the SERDES pin, these conditions are shown in the figure below.

CAUTION—The SERDES must tolerate a large data invalid window generated by the SONET framer ASIC, leaving only a small timing window for SERDES input uncertainty.

Figure 9-4: SERDES input waveforms at SERDES pin, i.e. transmit direction. 311 MHz transmit clock.



TXCLK will meet the duty cycle and rise/fall time specifications in the table. TXDATA will meet the rise/fall time specifications.

REFCLK will meet the rise/fall time and duty cycle specifications in table 9-4.

CENTERING CLOCKS. Unlike the 622 MHz mode, swapping clock inputs will not center the clock in the data bit. Thus, the SERDES must provide a delay in the clock path. To accomadate this, additional setup/hold time margin is budgeted (contrast TS, TH values for 311 MHz and 622 MHz mode).

Table 9-5: SERDES Input Timing Parameters, for 311 MHz clock mode.

PARAMETER SYMBOL	DESCRIPTION	VALUE
T0 (see figure)	clock period	1/(311.04 MHz) ~ 3.215ns
TW/T0	duty cycle = high going clk pulse width divided by clk period	0.48 < TW/T0 < 0.52 [1]
TR, TF	20-80% rise, fall times	100 - 300 ps
TS, TH [2]	setup time, hold time. defines data valid window with respect to clock at SERDES pin	1100 ps, 500 ps
T_dib, T_dia (see figure) [3]	defines data invalid window with respect to clock at SERDES pin	500 ps, 500 ps

[1] duty cycle is tight because the SONET framer ASIC output flop is clocked by same edge of TXCLK_SRC.
[2] Using setup/hold time terminology is a standard way of defining receiver input timing.
Assume 50/50% duty cycle for determining these timing values; duty cycle distortion is accounted for separately (see Sample Budget in Appendix).
[3] T_dib - time of data invalid before. T_dia - time of data invalid after. T_dib and T_dia provide an equivalent way of defining TS and TH in which the variables are mirrored around the clock edge.

9.5 SONET FRAMER input

Figure 9-5: SONET Framer input pin waveforms, i.e. receive direction.

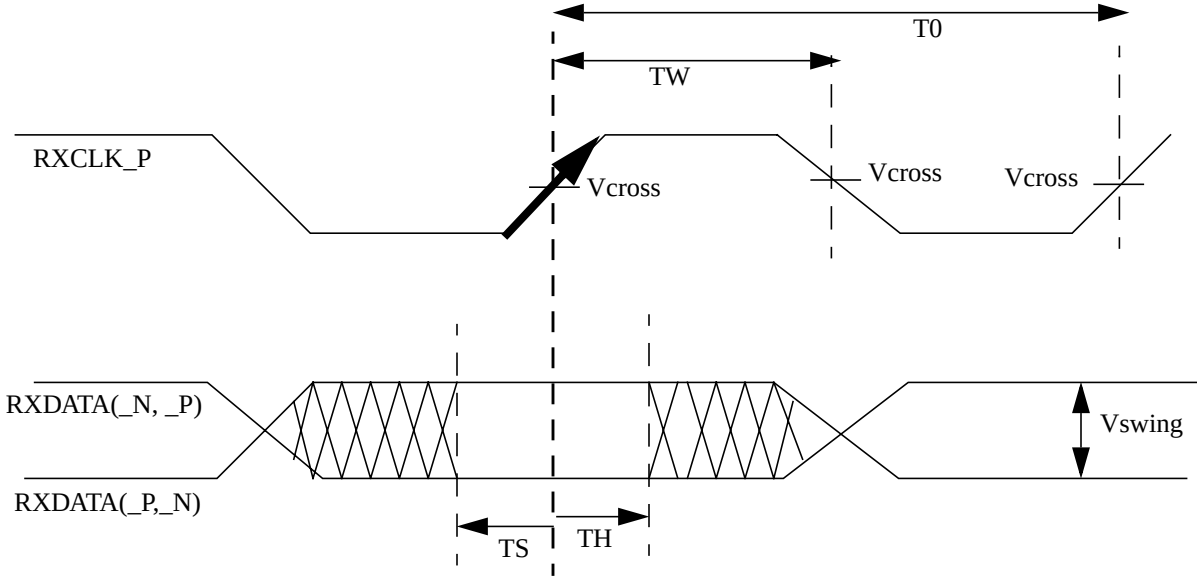


Table 9-6: Framer Input Timing Parameters, defined at Framer pin.

PARAMETER SYMBOL	DESCRIPTION	VALUE
T0 (see figure)	clock period	1/(622.08 MHz) ~ 1.608ns
TW/T0	duty cycle = high going clk pulse width divided by clk period	0.45 < TW/T0 < 0.55
TR, TF	20-80% rise, fall times	100 - 300 ps [1]
TS, TH	setup time, hold time. defines data valid window with respect to clock at Framer pin	300 ps, 300 ps

[1] Note that this range assumes a nominal 100 Ohm termination (does not include reflections).

These setup and hold times need to account for at least the following:

- mismatch between the receiver propagation delay for data vs. clock, over process, voltage, temperature
- wiring mismatch in the data vs. the clock paths
- setup and hold requirement of the latch on the Framer ASIC.

Package length mismatch can be adjusted for separately by compensating board etch lengths.

9.6 SONET Framer Output, Two Clock Modes

Two clock modes exist.

In the 311 MHz clock mode, the SONET framer ASIC transmits a 311.04 MHz clock along with the data. In the 622 MHz clock mode, the SONET framer ASIC transmits a 622.08 MHz clock along with the data.

NOTE— It is a REQUIREMENT that the 622 MHz clock mode be supported. It is highly recommended, but not required, that both the 311 MHz and the 622 MHz modes be supported, in order to maximize compatibility with other vendors' parts.

9.7 SONET Framer Output, Required 622 MHz Clock Mode

NOTE— In the 622 MHz clock mode, the SONET framer ASIC transmits a 622.08 MHz clock along with the data.

Note that for the 622 MHz clock mode, the values are relaxed since the data and the clock operate at different frequencies and delays are more difficult to match.

Figure 9-6: Framer output waveforms at Framer pin, i.e. transmit direction.

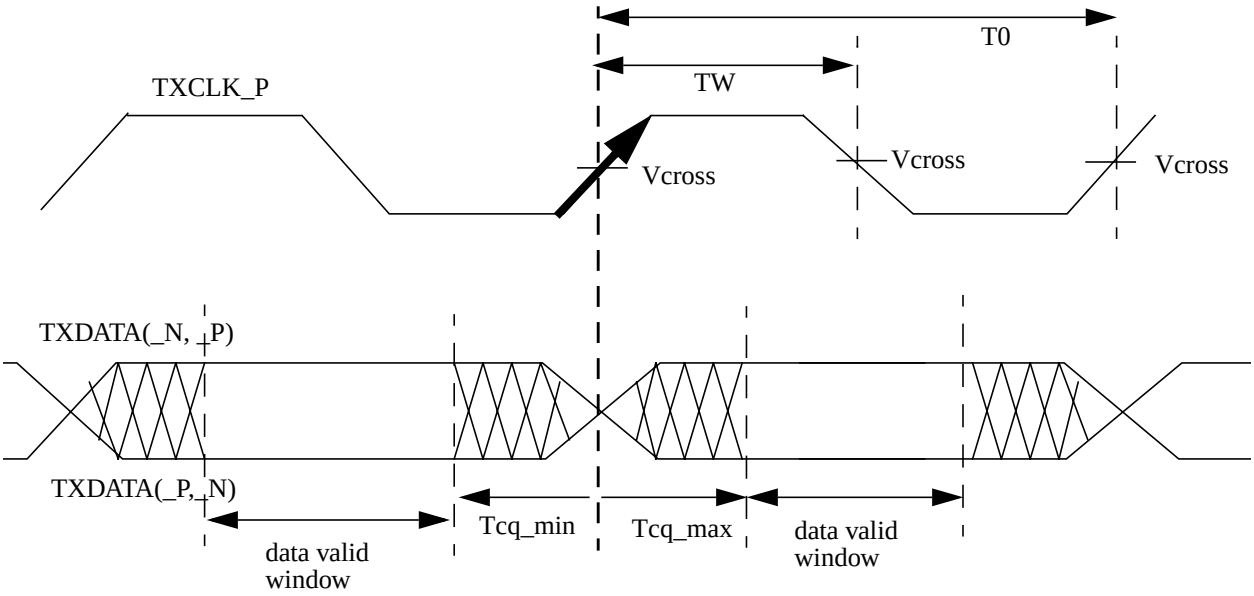


Table 9-7: FRAMER Output Timing Parameters, for 622 MHz clock mode, at Framer pin.

PARAMETER SYMBOL	DESCRIPTION	VALUE
T0 (see figure)	clock period	1/(622.08 MHz)
TW/T0	duty cycle = high going clk pulse width divided by clk period	0.4 < TW/T0 < 0.6 [1]
TR, TF	20-80% rise, fall times	100 - 250 ps
Tcq_min, Tcq_max (see figure)	defines data invalid window with respect to clock edge	200 ps, 200ps

[1] Note that this duty cycle is required even when TXCLK_SRC duty cycle is varied across its allowable range as specified earlier.

9.8 SONET Framer Output, 311 MHz Clock Mode

NOTE— In the 311 MHz clock mode, the SONET framer ASIC transmits a 311.04 MHz clock along with the data. The data bits are driven on both edges of the 311 MHz clock.

The data is transmitted from the SONET framer ASIC with a given clock-output uncertainty. When observed at the Framer data output pin with respect to the clock output pin, the clock to output delays permitted over process, voltage, temperature are shown in the following table. Also shown, are the duty cycle requirements that must be met at the Framer pin.

Figure 9-7: Framer output waveforms at Framer pin i.e. transmit direction. 311 MHz transmit clock.

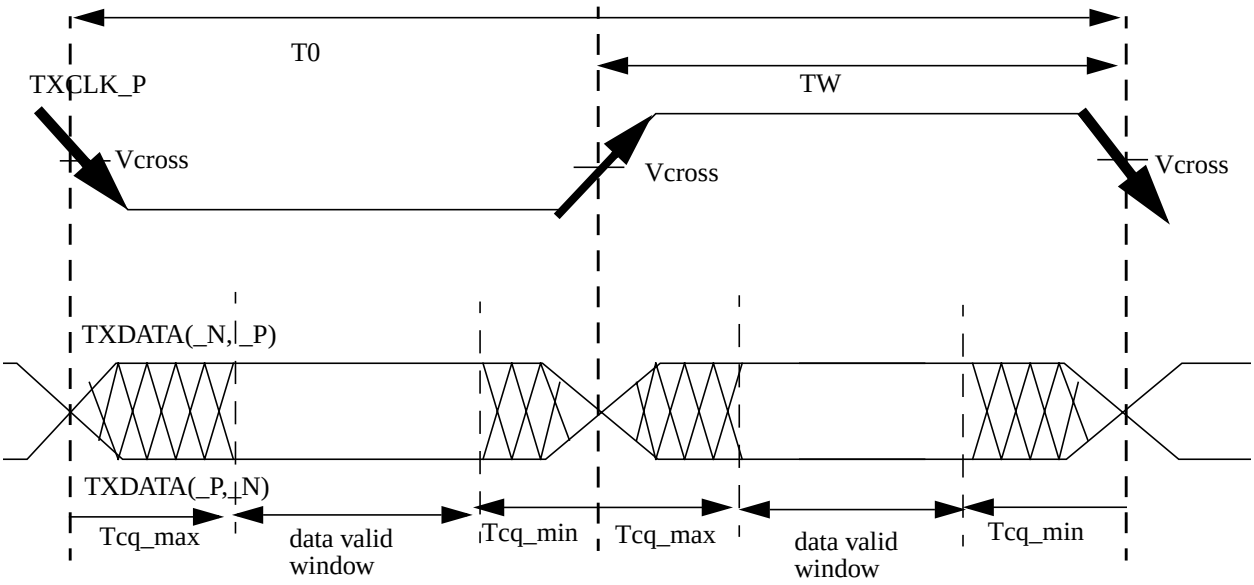


Table 9-8: Framer Output Timing Parameters, for 311 MHz clock mode, at Framer pin.

PARAMETER SYMBOL	DESCRIPTION	VALUE
T0 (see figure)	clock period	1/(311.04 MHz) ~ 3.215ns
TW/T0	duty cycle = high going clk pulse width divided by clk period	0.48 < TW/T0 < 0.52
TR, TF	20-80% rise, fall times	100 - 250 ps
Tcq_min, Tcq_max (see figure)	defines data invalid window with respect to clock edges	200 ps, 200ps

10. Summary

This document described SFI-4, the electrical interface between STS-192/STM-64 framers and the Serializer/Deserializer for tranfer of data.

This document includes the signal definitions, function, timing, clocking, and signal levels. It does not include the mechanical or environmental specifications. Also, it does not specify signals beyond the scope of this interface, even though they might be present in a module that includes this interface.

11. References

“LVDS standard.” IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), IEEE, NY, NY, 7/31/ 96.

“GR-1377.” Bellcore Generic Requirements, GR-1377-CORE, Issue 5, 12/98, Sonet OC-192 Transport System Generic Criteria.

“G.783.” ITU-T Recommendation G.783 (04/97) CHARACTERISTICS OF SYNCHRONOUS DIGITAL HIERARCHY [SDH] EQUIPMENT FUNCTIONAL BLOCKS.

12. Appendix A: Sample Timing Budgets - Informative

This appendix is meant to be informative, not normative.

12.1 Sample timing budget in receive direction

The SERDES sends data to the Framer. The calculations below assume a conservative linear addition of timing error sources. Assume timing is observed at the receiver input.

Table 12-9: Timing, receive direction

DESCRIPTION	VALUE (+/-)
driver timing error [1]	200ps
module timing error [2]	50ps
receiver timing error [3]	300ps
duty cycle distortion, if clocks swapped [4]	80ps
leaves this much for jitter [5]	170ps
BUDGET [6]	TOTAL: 800ps

[1] driver timing error - from section on SERDES timing. See section below.
[2] module timing error - assume another 50ps error accounts for such effects as module length mismatch, connector length mismatch, skew induced by module and connector noises (reflection, crosstalk)
[3] receiver timing error - from section on Framer timing. See section below.
[4] duty cycle distortion - assumes that to achieve centering of the clock in the data bit, the clock inputs are swapped on the board. Since the driver uses the rising clock edge, whereas the receiver would use the inverted falling clock edge, duty cycle must be considered. A 45-55% duty cycle causes a jitter of +/-5% of 1600ps. Alternately, can use discrete delay line, to reduce this value.
[5] “leaves this much for jitter” - System designer can allocate the skew remaining to fill the 800ps budget as needed for the specific system implementation. For a list of jitter sources that are typically of concern, see “Jitter sources” below.
[6] The clock is used to trigger on the data eye of 1600ps width, i.e. +/- 800ps.

12.2 Sample timing budget in transmit direction, 622 MHz mode

The Framer sends data to the SERDES. The calculations below assume a conservative linear addition of timing error sources. Assume timing is observed at the receiver input.

Table 12-10: Timing, transmit direction, 622 MHz mode.

DESCRIPTION	VALUE (+/-)
driver timing error [1]	200ps
module timing error [2]	50ps
receiver timing error [3]	300ps
duty cycle distortion, if clocks swapped [4]	160ps
leaves this much for jitter [5]	90ps
BUDGET [6]	TOTAL: 800ps

[1] driving timing error - from section on Framer timing
[2] module timing error - assume another 50ps error accounts for such effects as module length mismatch, connector length mismatch, skew induced by module and connector noises (reflection, crosstalk)
[3] receiver timing error - from section on SERDES timing
[4] duty cycle distortion - assumes that to achieve centering of the clock in the data bit, the clock inputs are swapped on the board. Since the driver uses the rising clock edge, whereas the receiver would use the inverted falling clock edge, duty cycle must be considered. A 40-60% duty cycle causes a jitter of +/-10% of 1600ps. Alternately, can use discrete delay line, to reduce this value.
[5] “leaves this much for jitter” - System designer can allocate the skew remaining to fill the 800ps budget as needed for the specific system implementation. For a list of jitter sources that are typically of concern, see “Jitter sources” below.
[6] The clock is used to trigger on the data eye of 1600ps width, i.e. +/- 800ps.

12.3 Sample timing budget in transmit direction, 311 MHz mode

The Framer sends data to the SERDES. The calculations below assume a conservative linear addition of timing error sources. Assume timing is observed at the receiver input.

Table 12-11: Timing, transmit direction, 311 MHz mode.

DESCRIPTION	VALUE (+/-)
driver timing error [1]	200ps
module timing error [2]	50ps
receiver timing error (incl. centering clock)[3]	300ps
duty cycle distortion [4]	60ps
leaves this much for jitter [5]	190ps
BUDGET [6]	TOTAL: 800ps

[1] driving timing error - from section on Framer timing
[2] module timing error - assume another 50ps error accounts for such effects as module length mismatch, connector length mismatch, skew induced by module and connector noises (reflection, crosstalk)
[3] receiver timing error - from section on SERDES timing. Note that the receiver timing error in the 311MHz clock mode, in contrast to the 622MHz clock mode, includes timing error due to centering the clock on the SERDES.
[4] duty cycle distortion - assumes that for the 311 MHz clock mode, the centering of the clock is done on the SERDES. So, in contrast to the 622 MHz clock mode, clock inputs need not be swapped. However, duty cycle distortion inherent in TXCLK is still +/-2% * 3200ps = +/- ~60ps.
[5] “leaves this much for jitter” - System designer can allocate the skew remaining to fill the 800ps budget as needed for the specific system implementation. For a list of jitter sources that are typically of concern, see “Jitter sources” in the following section. **Note that 311 MHz mode allows more jitter.**
[6] The clock is used to trigger on the data eye of 1600ps width, i.e. +/- 800ps.

12.4 Timing errors

12.4.1 Driver timing error

The driver timing error includes on-chip and package timing errors. This includes variations in arrival times of any data output relative to the clock output, measured at the output package pins. This is measured over process, voltage, temperature. Error sources include

1. propagation delay differences between the data and clock paths due to different active elements (buffers, flops) in data and clock paths
2. wire delay differences in the data and clock paths
3. wire delay differences between data bits
4. different loading in the data and clock paths
5. package length differences

To simulate the driver in HSPICE, assume an input clock of ideal duty cycle, and apply to the circuit and package models, which include extracted parasitics. Terminate with an ideal 100 Ohm resistor. Observe arrival times of the data vs. clock edges over process, voltage, temperature, and data patterns (ex. 1010, 1110, 0001).

12.4.2 Receiver timing error

The receiver timing error includes package and on-chip timing errors as well as the setup/hold time at the flop. This includes variations in times of any data relative to the clock, measured at the flop input. This is measured over process, voltage, temperature. Error sources include

1. propagation delay differences between the data and clock paths due to different active elements (buffers) in data and clock paths
2. wire delay differences in the data and clock paths
3. wire delay differences between data bits
4. different loading in the data and clock paths
5. package length differences
6. nominal delay error and delay variations due to centering the clock relative to the data bits. On-chip centering is required for the 311 MHz. It is not required for the 622 MHz mode, for which clock inputs may be swapped.
7. setup and hold time requirements

To simulate the receiver in HSPICE, assume a minimum swing LVDS input of ~200ps rise and fall time, Apply to the package and receiver models, which include extracted parasitics. Terminate with a typical capacitive on-chip load. Observe arrival times over process, voltage, temperature. Add in setup and hold times.

12.4.3 Jitter Sources

Listed below are examples of jitter sources.

Table 12-12: List of sample jitter sources.

CATEGORY	JITTER SOURCES
ISI (intersymbol interference)	[1]
reflection noise skew	skew due to termination resistance mismatch [2]
	skew due to package impedance mismatch
	skew due to connector and module impedance mismatch [3]
	true/complement length mismatch skew [4]
switching noise skew	on-chip switching noise, from driving and receiving chips [5]
crosstalk skew	driver and receiver package crosstalk skew
	connector crosstalk skew
	board and module trace crosstalk skew
power supply noise skew	[6]
common mode skew	[7]

[1] ISI is severe in bandwidth limited channels (e.g. attenuating board traces), where a 0101 pattern will produce different threshold crossings than a 1110 pattern.
[2] termination resistance mismatch -
* If on-chip termination, skew due to mismatch in termination resistance.
* If external termination, skew from reflection at the termination stubs.
* A special case of this is resonance of the clock line. Depending on board trace length chosen, multiple reflections may add destructively/constructively.
[3] connector and module impedance mismatch - skew from this has already been accounted for in the foregoing budgets under “module skew”. repeated here for completeness.
[4] true/complement length mismatch - The package length for the True signal may not be equal to that of the Complement signal. Even if the delay is compensated by adding board trace delay, reflections do not line up.
[5] switching noise - causes noise that when received, may convert to skew. Also, may modulate driver and receiver propagation delays.
[6] power supply noise skew - power supply noise may modulate driver and receiver propagation delays.
[7] common mode skew - mentioned here, though this is not strictly jitter source. Receiver propagation delay is a function of common mode voltage. The receiver propagation delay may vary depending on what actual common mode voltage is chosen.

12.4.4 System simulation and measurement

In addition to the simulation and measurement of the driver and receiver in isolation, the system designer must simulate and measure the driver and receiver together. A representative environment should be chosen, including connector and module trace models. This will allow closer investigation into jitter sources (see following section on “Sample Jitter Sources”) that arise from interoperating the drivers and receivers. Intersymbol interference and reflection simulations are strongly encouraged.