300-mm Monolithic Silicon Photonics Foundry Technology

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(Invited Paper)

***Abstract*—A competitive 300-mm silicon photonics foundry technology has been developed by GLOBALFOUNDRIES for general availability, which takes advantage of advanced CMOS process technology and provides a manufacturing scale. A state-of-the-art process design kit offers a codesign environment with access to a comprehensive photonics device library along with a monolithically integrated SOI CMOS device library. Advances in automated wafer-level optical test enable statistical photonic device characterization for development, photonic modeling, and manufacturing controls. The key challenges and solutions in developing a manufacturable photonic technology with state-of-the-art performance are described, as well as a roadmap for next generation high-performance monolithic silicon photonics are outlined.**

***Index Terms*—Silicon photonics, monolithic CMOS, 300 mm foundry.**

I. Introduction

THE demand for silicon photonic solutions continues to grow with volumes driven by transceivers for Data Center Interconnect (both intra-DCI and inter-DCI), 5G backhaul/fronthaul, metro/long haul datacom and telecom, and passive optical networks. In addition to these established applications, there is a growing demand to develop silicon photonics for new product applications that include chip-to-chip electrical/optical interconnect, automotive LiDAR (light based radar), high performance computing (Artificial Intelligence, Quantum Computing), and infrared imaging and sensing.

To address this market expansion, GLOBALFOUNDRIES has qualified a 300 mm silicon photonics foundry technology offering, CMS90WG, which leverages state-of-the-art CMOS manufacturing processes and enables optical product designs with comprehensive O and C-band photonic device libraries with an option to monolithically integrate 90 nm SOI RF CMOS active and passive circuitry for analog and digital control. Key photonic devices include Silicon-on-Insulator (SOI) and silicon nitride waveguides, high bandwidth Mach-Zehnder modulator (MZM) and Ge epitaxy photodiode, low loss passive aligned fiber attach, coarse Wavelength Division Multiplexing (cWDM), high efficiency isolated thermal phase-shifters, RF passives, ESD protection, e-fuse embedded memory, and a standard cell digital library. A fully enabled Cadence design kit provides an electrical and optical co-design and co-simulation environment which includes p-cell layouts, Verilog-A compact models, Calibre design-rule checking, layout vs schematic, and parasitic extraction tools. Custom photonics designs can also be submitted on a curve-linear format with use of recently developed freeform design enablement.

The manufacturing process leverages 300 mm immersion lithography and optical proximity correction (OPC) for waveguide patterning levels to optimize loss and device performance across a wide range of device structures. Critical process steps such as Ge EPI growth, modulator implants, recess reactive ion etch (RIE), and film depositions are controlled using best-known-methods as developed for advanced node 300 mm CMOS manufacturing. Inline wafer level electrical and optical device testing is deployed using automated inline wafer-level testing across the key devices offered which is used to apply an outgoing wafer acceptance criteria (WAC) against both electrical and optical device parameters.

This paper will expand on the key challenges and solutions applied to develop a manufacturable monolithic photonic technology which spans areas of process integration, patterning, device design, test, design enablement and reliability. Some highlights of the development roadmap will also be discussed.

Manuscript received December 5, 2018; revised February 26, 2019; accepted March 27, 2019. Date of publication April 1, 2019; date of current version April 23, 2019. *(Corresponding author: Ken Giewont.)*

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Digital Object Identifier 10.1109/JSTQE.2019.2908790

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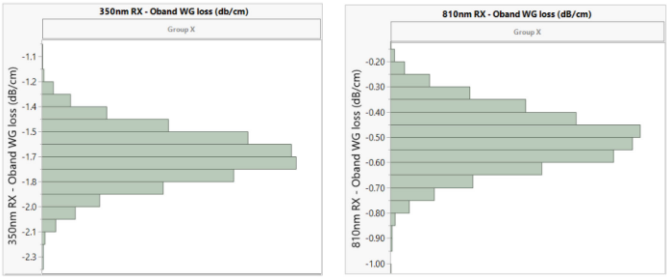


Fig. 1. Distribution of SOI waveguide propagation loss on recent lots in manufacturing. Single mode (350 nm wide) SOI waveguide represented on left, and Multi-mode (810 nm wide) SOI waveguide represented on the right.

TABLE I
COMPARISONS OF CD SIGMA AND LER FROM DRY LITHOGRAPHY AND IMMERSION LITHOGRAPHY IN 300 mm FACILITY

	Dry Lithography		Immersion Lithography	
Features	CD sigma (nm)	LER (nm)	CD sigma (nm)	LER (nm)
150 nm ridge waveguide	0.99	6.4	0.32	3.5
350 nm ridge waveguide	0.87	6.8	0.4	3.8
400 nm ridge waveguide	0.94	6.1	0.31	3.3

II. WAVEGUIDES

The CMS90WG technology platform offers full-height and partially-etched silicon waveguides (ridge and rib respectively), with the option to support single- and multi-mode operation by adjusting the waveguide width. Using advanced 300 mm lithography and etch processes we have demonstrated ridge waveguides with single-mode propagation losses better than 1.5 dB/cm (Fig. 1). Further improvements are in development. The introduction of immersion lithography and the appropriate resist systems has provided a significant reduction in line edge roughness (LER) and corresponding waveguide loss. Table I shows up to a 67% improvement in critical dimension (CD) sigma for the 150 nm ridge case when moving from dry lithography to immersion lithography with the appropriate resist system. In addition to the reduction in loss, an improvement in process tolerance is observed for both the ridge and rib waveguides due to the improved etch processes. In addition to waveguide patterning, significant improvements in waveguide loss have been obtained by reducing residual metallic components from the silicide process. Implementation of an improved silicide cleaning process resulted in a reduction in loss of >1 dB/cm as shown in Fig. 2.

Further reduction in waveguide loss is possible by working with wafer vendors to improve the incoming wafer properties, as well as optimizing the integrated process flow. Low-loss waveguides for wavelength regimes including C- and L-bands are presently under development. Additionally, as part of a foundry silicon photonics roadmap, a CMOS integrated low loss silicon nitride waveguide ($<$0.3 dB/cm) has been demonstrated.

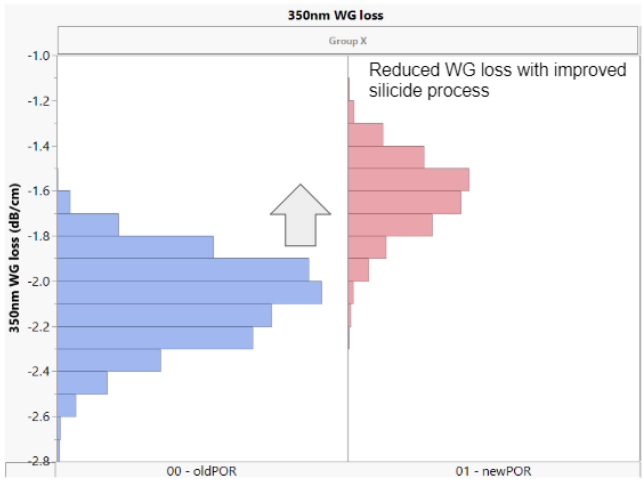


Fig. 2. Improvement in propagation loss with modification to the silicide process to remove metallic. Cell 00 "oldPOR" refers to original process of record. Cell 01 'newPOR" refers to improved process of record.

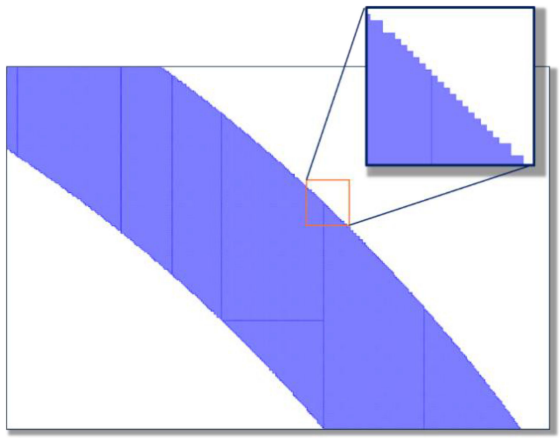


Fig. 3. Layout image of a portion of a waveguide. Note that the curved border of waveguide is composed of very small horizontal and vertical edge fragments.

The addition of a nitride waveguide into the foundry platform opens up options for the design of new high performance active and passive optical components.

III. OPTICAL PROXIMITY CORRECTION

Most Optical Proximity Correction (OPC) tools developed for traditional CMOS structures are designed to best handle orthogonal "Manhattanized" design styles where the target design polygons are drawn using vertical and horizontal edges in the incoming GDSII layout. When adapting these OPC recipes to curved photonics structures like waveguide bends, one obvious approach is to Manhattanize the incoming curved design with a series of very small stair-steps, closely approximating the curve with short vertical and horizontal edge components as shown in Fig. 3. This approach is fairly simple and effective, and can be carried all the way from design to mask – providing relatively few challenges for tool designs to work on this kind of layout. The result is friendly to mask fracture and mask write processes,

and provided the step size used is small enough, the resulting images patterned in photoresist can retain their smoothed curved nature. Lithography cannot resolve the very small jogs and corners on these kinds of Manhattanized OPC solutions because the photoresist imaging process acts as a low-pass filter blurring the image to very closely match the design intent.

There are some short-comings associated with the Manhattanization approach to OPC. First, it adds a step to the design to mask flow which either forces the designer to drawn the target shapes in Manhattanized form, or to convert curvilinear layouts to a Manhattanized form. In many instances the designer would prefer not to do this – as the smooth curvilinear layout most accurately represents the intended wafer target shapes. There is also concern about loss of accuracy caused by approximation of a curved structure with a series of small stair steps. Another challenge with Manhattanized OPC flows is the need to correct for etch process biases, oxidation step and other processing steps after the lithography step which can cause the final structure to deviate from the final wafer target dimension.

Many traditional OPC recipes have rules-based correction recipes designed to compensate for these post-lithography processing steps using space and width dependent rules. Measuring width and spaces on non-rectangular geometries can be fairly complex, as the notion of "width" on a curved waveguide becomes difficult to measures on a Manhattanized representation.

In response to the above challenges, we have developed an OPC mask correction flow that can read in a smooth curved representation of photonics structures in oasis or GDSII format, and which outputs similar smooth curves for mask fracture. This free-form OPC correction flow involves three stages of correction which compensate for oxide deposition, etch biases and optical proximity effects. At each stage of correction, we build models based on measurements made on special test patterns printed on wafers and measured at the corresponding stages of wafer processing. We validate these models by testing them on patterns not used for calibration, comparing the final post-OPC mask shapes to ones obtained using a traditional Manhattanized OPC flow. We also use well established lithography simulation tools to compare the expected printed contours in photoresist using XOR methods on a wide variety of photonics layout. In most instances the results from the two flows have been found to match closely, though in some cases, investigating XOR differences has revealed small short-comings in the Manhattanized approach. We are currently in the process of qualifying the free-form OPC approach using optically testable photonics devices to verify that the optical performance is indeed equal to or better than with the Manhattanized approach.

IV. Modulators

The CMS90WG platform enables photonic transmitters built from a monolithically integrated travelling wave Mach-Zehnder modulator (TW MZM) coupled with CMOS drivers capable of non-return to zero (NRZ) modulation above 25 Gb/s [1]. The CMS90WG physical design kit (PDK) offers a 10 Gb/s MZM with a minimum 14 GHz small-signal electro-optical bandwidth, a 6.3 dB extinction ratio, and a −3.8 dB optical loss and a 25 Gb/s

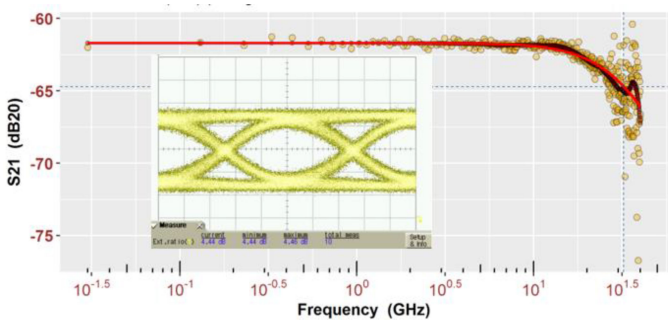


Fig. 4. The electro-optical response of a 50 Gb/s TW MZM was characterized as previously outlined[5]. The quoted bandwidth (>35 GHz) reflects the frequency at which a low-pass filter curve (red line) passes 3 dB below the maximum value of the spline fit curve (black line). The NRZ eye diagram (inset) reflects a 2^{31}-1 pseudo-random bit stream pattern. The median eye opening gives an RF extinction ratio of 2.3 dB.

MZM with better than 20 GHz bandwidth, a 2.3 dB extinction ratio, and a −2.1 dB optical loss.[1] Fig. 4 shows the electro-optical response of a 50 Gb/s MZM presently under qualification. This design demonstrates >35 GHz bandwidth, a 2.6 dB extinction ratio, and −4.0 dB optical loss. Previously, a monolithic 4-level pulse-amplitude modulation (PAM4) transmitter has shown 56 Gb/s operation [2] and hybrid solutions with segmented MZMs and off-chip drivers have also been reported [3], [4].

Transmitters with high bandwidth and low drive power are essential for efficient short reach link performance. For a given MZM design, there is a trade-off between optical loss, extinction ratio, and bandwidth. The first two elements can be lumped together and expressed as a relative optical modulation amplitude (ROMA) or combined with the bandwidth to create a single figure of merit [5]. Fig. 5 illustrates the substantial impact in optical modulation and bandwidth from changes in the location of activated carriers (MZM-A to MZM-B to MZM-C). Also shown is the impact of reduced carrier dose for a given design (e.g., MZM-C to MZM-C low). This two-dimensional view of the modulator performance space has been used to screen candidate MZM designs that meet a threshold bandwidth (e.g., 70% of the target bitrate) and to optimize implants for each design.

These MZMs benefit from several elements of an integrated CMOS technology: SOI waveguides for improved isolation and reduced impedance, low-energy ion implantation for optimized modulator performance and precision broadband resistors, metal silicide for thermal heaters, and advanced silicon patterning for control of waveguides and couplers. They are highly manufacturable due to excellent broadband performance and

[1]Bandwidth is quoted at 3 dB below peak signal with oversampling and low-frequency filtering applied (see Fig. 4 for details). The extinction ratio reflects the median eye opening for a '11110000' pattern run at 25 GHz. The eye opening for a $2^{31}-1$ pseudo-random number pattern run at the same frequency is slightly smaller due a mismatch between the impedance of the modulator (about 30 ohm) and the output impedance of the test bench driver (50 ohm). The 10 Gb/s MZM was measured at 1.0 V reverse junction bias with a 2 V Vpp (4V Vppd) drive. The 25 Gb/s and 50 Gb/s MZMs were measured with a 0.5 V reverse junction bias and a 1 V Vpp (2 V Vppd) drive. Test equipment to drive the 50 Gb/s MZM above 35 GHz was not available at the time of measurement.

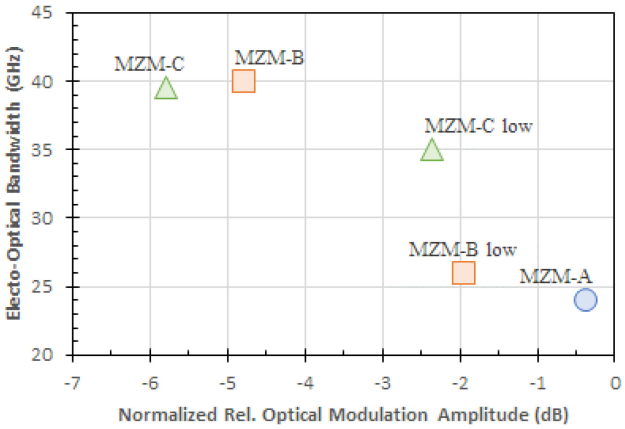


Fig. 5. The relationship between electro-optical bandwidth and relative optical modulation amplitude (ROMA) is explored across several modulator designs (MZM-A, MZM-B, MZM-C) and by modifying the implant dose (MZM-B low, MZM-C low). *Note that the ROMA quoted in this figure has been normalized relative to an arbitrary value.*

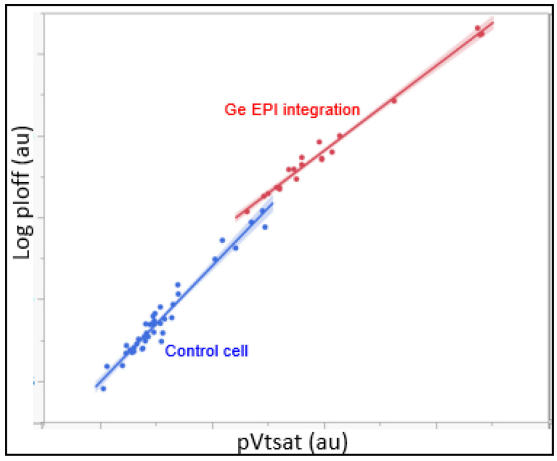


Fig. 6. pMOS Vtsat vs Ioff for control cell and first experiment with Ge EPI integration. The experiment cell showed a significant shift in both parameters.

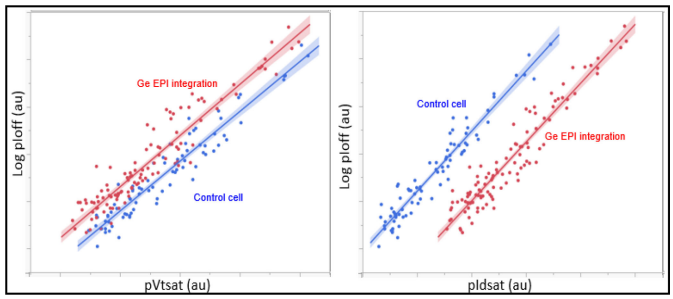


Fig. 7. pMOS performance (Vtsat & Idsat vs Ioff) for control and Ge EPI cells. Improved Idsat for experimental cell was due to device adjustments.

relatively good temperature stability. However, they employ large-area junction phase shifters that require traveling wave (or segmented) electrode designs in order to operate at high frequencies. Lumped-element ring modulators have a much smaller footprint and are very efficient at RF driver power consumption. However, ring modulators are rather temperature sensitive and require a viable thermal stabilization strategy. Heaters that have been undercut to substantively remove the substrate have much lower power draw and may be required to make ring modulators a competitive option [6]. Compact transmitter designs incorporating integrated inductors into the MZM electrode have also been demonstrated [7].

V. Ge Photodetector

A lateral Germanium (Ge) epitaxy (epi) photodiode (PD) is integrated into the CMS90WG monolithic CMOS process flow which offers high performance operation for O-band and C-band applications while also maintaining CMOS FET performance characteristics. Significant process optimization was required to define and qualify the final process due to several thermal constraints which included low Ge melting temperature (938 °C), minimum epi temperature for high quality Ge and the high sensitivity of the CMOS device performance to thermal budget.

The epitaxially grown Germanium film was fabricated using advanced tooling common to leading edge scaled CMOS manufacturing flows. A selective growth process was utilized which forms an epi film in a shallow cavity partially recessed within the SOI waveguide. The photodiode design includes a lateral PIN structure where the p-doped and n-doped regions are contacted through heavily doped regions in the SOI layer with Tungsten contacts outside the Ge on silicided silicon [8]. This process is integrated in the flow after the high temperature (>950 °C) CMOS activation anneal to avoid Ge film recrystallization and before the CoSi silicide process. The epi growth temperature was found to be a critical parameter which required several rounds of process experiments to select the final condition. A temperature between 750–800 °C was favorable for reducing threading dislocations [9] and producing a high quality crystalline film. However, this growth temperature was found to significantly degrade the CMOS PFET performance as shown in the Ioff vs Vtsat plot in Fig. 6. This was attributed to Boron diffusion during the relatively high temperature (800 °C) process used in the Germanium photodiode fabrication.

This lead to further development of a low temperature (<750 C) epi growth process which minimized the impact to the CMOS devices performance, prevented doping deactivation [10] while also producing a high quality crystalline Ge film. In order to mitigate the impact of the lower thermal budget, additional improvements had to be made to the process which ranged from optimizing key steps like bakes, cleans, growth temp, as well as diode implant conditions.

The final Ge epi process integration conditions demonstrated improvement of the CMOS PFET performance (higher Idsat drive current for a given Ioff current) as shown in Fig. 7 while also enabling a high performance photodiode. The final process developed demonstrated reverse bias (−1 V) dark currents ranging from 35–70 nA, responsivity of approximately 1.0 A/W and an analog bandwidth of approximately 40 GHz as shown in Figs. 8 and 9 respectively. The combined set of results of matched or improved CMOS performance with a high performance photodiode paved the way to enable a full monolithic CMS90WG Silicon Photonics offering.

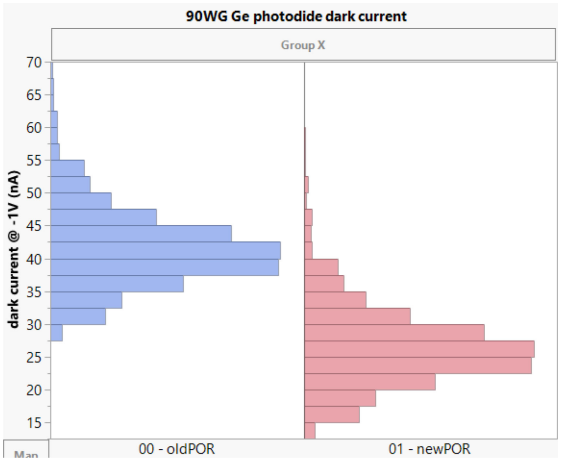


Fig. 8. Distributions of Ge EPI PIN dark current @ −1V for oldPOR and newPOR. The latter cell is the lower thermal budget solution.

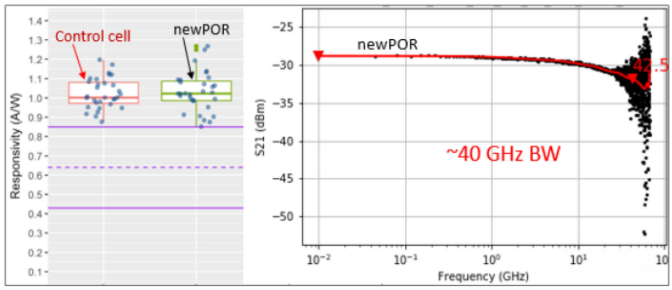


Fig. 9. Responsivity (A/W) and bandwidth measured at −1.2 V, newPOR process showing ∼1 A/W responsivity & 40 GHz bandwidth.

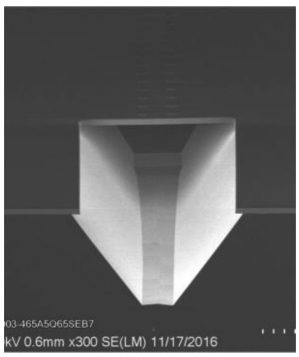


Fig. 10. Perspective view electron micrograph of the fiber-to-chip interface with integrated V-groove and suspended mode converter for large mode expansion.

Further optimization of the Ge module is possible. Ge epi growth, implants and pre-clean conditions have been defined which demonstrate a path to analog bandwidths in the range of 50–60 GHz with minimal penalty to responsivity and dark current.

VI. Fiber to Chip Interface

The fiber-to-chip interface is shown in Figs. 10 and 11. To enable low-cost packaging, the interface includes a fiber V-groove

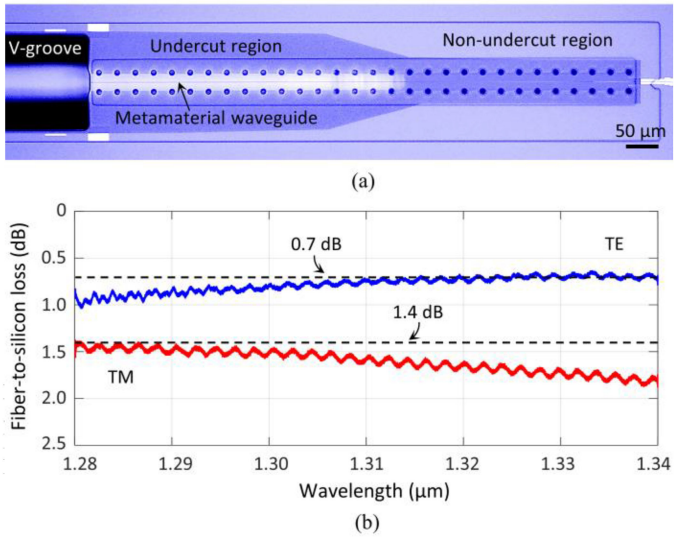


Fig. 11. Fiber-to-chip interface with integrated V-groove and suspended mode converter for large mode expansion. (a) Top down optical micrograph (b) Transmission ls from standard, cleaved, self-aligned fiber to a routing Si waveguide.

integrated on chip with full mode expansion. The V-grooves self-align standard cleaved fibers to integrated fiber couplers, which match the standard 9–10 μm fiber mode with sub-decibel mode overlap loss. No active-alignment or expensive in-fiber mode conversion is needed.

The mode expansion to a full fiber mode is achieved with a silicon metamaterial converter embedded in a thick, suspended oxide membrane. The silicon handle wafer is removed below the converter to prevent optical leakage of the large mode to the silicon substrate. The metamaterial waveguide employs periodic silicon structures of too small a pitch for diffraction to occur. It acts on the optical wave as a continuous, engineered optical material. The concept is similar to the subwavelength grating coupler of [11]. In addition to enabling better design flexibility, it was shown in [12] to provide better fabrication tolerances than typical inverse tapers. The first demonstration of this interface in a CMOS production facility was reported in [13]. A peak performance of −1.3 dB was achieved with 0.8 dB penalty over a 100 nm spectrum and all polarization, although with a significant TE reflection of −16 dB. The device reflection was recently improved to −35 dB [11]. The new spectral response is shown in Fig. 11(b). A peak transmission of −0.7 dB is found on TE. A 0.7 dB excess loss is found on TM and was attributed to a non-optimal section in the non-linear taper, which is being currently corrected. Regular monitoring of the device shows we can consistently achieve better than 1.5 dB insertion loss for TE and TM in a manufacturing process flow.

VII. V-Groove Integration With CMOS

As described above, we have successfully integrated a V-groove structure for passive alignment into a 300 mm foundry manufacturing processes.

To enable this V-groove technology on a 300 mm manufacturing scale required some significant changes to best known

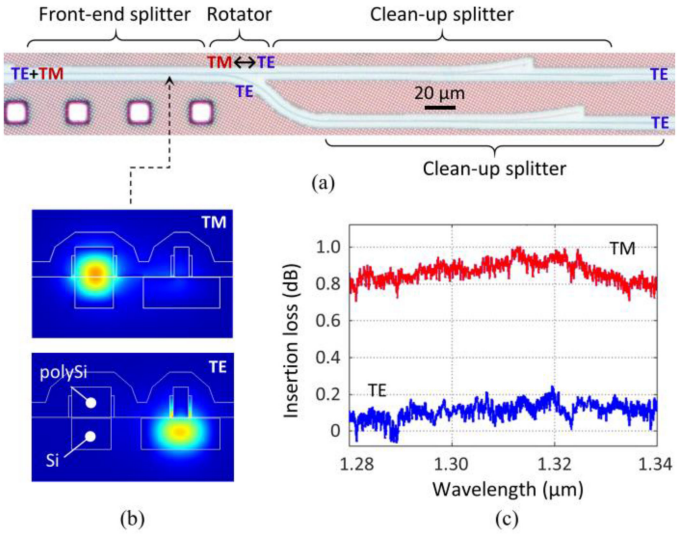


Fig. 12. Integrated polarization splitter and rotator implemented as a two-layer mode-evolution device. (a) Top-view optical micrograph. (b) Field intensity of main modes near the end of the splitter. (c) Loss spectrum dominated by mode overlap with lossy polysilicon

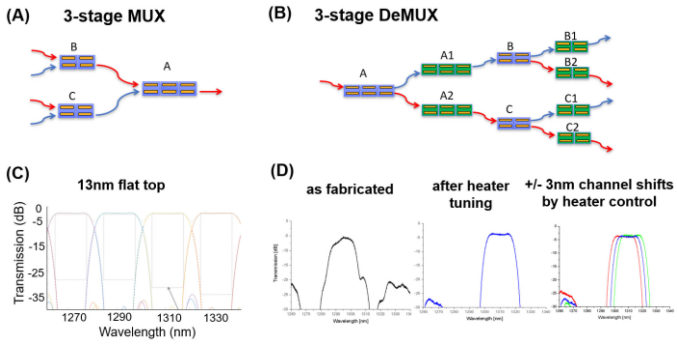


Fig. 13. cWDM design and tested results. (A, B) schematics of 3-stage MUX and DeMUX. (C) Simulated cWDM with experimental extracted parameters. Loss per channel is 2.2 – 2.7 dB and cross talk is below −23 dB. (D) Experimental demonstration of a single channel.

methods. As CMOS moved to smaller nodes, the focus was to improve patterning capability, primarily improving small patterns on flat wafers. Photonics and the addition of a V-groove change this dynamic, requiring processes that can pattern images over very large topographies. In order to cover these large steps ($>$13 μm thick), 10 μm resists were employed which then challenges the alignment systems and depth of focus in the current lithography tools. Etching these deep structures also requires longer more uniform etch processes to obtain the desired control of the fiber placement and low loss. These long etches need to be carefully designed to protect the wafer edge and avoid any arcing or charging problems during etch.

A tetramethylammonium hydroxide (TMAH) etch module has been developed to create the deep, crystallographic etch which aligns the fiber center to the coupler waveguide, providing consistent low loss fiber attach. Fig. 10 shows an electron micrograph of the final V-groove structure used for passive fiber attach.

VIII. Polarization Management

Integrated polarization management is key to wavelength division multiplexing receivers and to transmitters and receivers of polarization multiplexed channels, as typically used with coherent detection schemes. A fundamental building block is a polarization splitter and rotator. As shown in Fig. 12, this device splits the TE and TM components of a mixed polarization state and rotates the split TM into TE. It also works in reverse direction by accepting two TE signals, rotating one into TM and combining the two signals into one waveguide.

The integrated polarization splitter and rotator employs a mode evolution design [14], [15] for wide spectral bandwidth and tolerances to fabrication offsets. It is a two-layer structure re-purposing the silicon on insulator and polysilicon gate layers for polarization management. The performance was reported in [16]. Over the 60 nm bandwidth measured, the polarization extinction was better than 27 dB and the loss was better than 1.0 dB. As shown in Fig. 12(b), the loss is dominated by material absorption in the polysilicon layer. This results in a larger loss on TM as induced by the stronger overlap of that mode with the lossy polysilicon layer.

IX. Coarse Wavelength Division Multiplexer (cWDM)

The wavelength division (de)multiplexer (WDM) is a critical building block for optical interconnects. A multiplexer joins multiple data streams together into one fiber, and a demultiplexer at the receiver splits them apart. cWDM systems enable expanded network capacity without the expense of additional fibers. In CMS90WG technology, a pcell is available for an O band cWDM device with four channels, centered at 1271, 1291, 1311, 1331 nm. The design is based on a binary tree of 1-to-2 Mach-Zehnder interferometer (MZI) filters [17], [18]. In order to achieve superior flat-top filter response, additional MZI stages are included in the lattice filter. As shown in Fig. 13(A-B), MUX and DeMUX designs use 2 and 3 stage MZIs as the basic lattice filter. The DeMUX repeats each filter stage for improved cross-talk. Fig. 13(C) shows the simulated results of DeMUX flat top channels, with 13 nm channel width. The simulated loss per channel is 2.2–2.7 dB, and cross talk is <-23 dB. Fig. 13(D) shows an experimental demonstration of one channel. A clean channel shape was formed after heater tuning protocol, with <-25 dB cross talk and 2.5 dB channel loss. In addition, we also demonstrated the control of channel positions (e.g., $+/-3$ nm) by tuning the heaters, as shown in the last figure in Fig. 13(D).

In order to reduce the power consumption of thermal phase tuning, we leveraged the CMS90WG unique substrate removal process and designed a thermal heater with undercut cavities, as shown in Fig. 14. The undercut cavity is formed by leveraging the same deep substrate etch that is used to create the fiber attach v-groove structure as described in Section VII. Substrate removal helps with thermal isolation and increases local heating temperature, and therefore, improves the thermal tuning efficiency [6]. Fig. 14(A) shows the optical top-down image of an

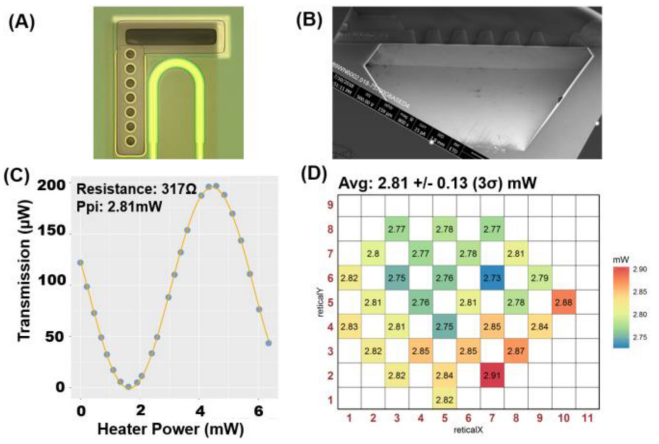


Fig. 14. Undercut heater. (A) Optical top-down image of an undercut heater. The rectangular dark shade indicates the undercut area of the handle wafer. (B) SEM cross-section of a cleaved V-groove cavity under heater. (C) Sine curve of optical power versus applied heater electrical power. Extracted power per pi phase shift is only 2.81mW, which is about 15× lower than non-undercut heaters. (D) Wafer map of the undercut heater power per pi. Heater tuning efficiencies is very uniform, ranging from 2.73 to 2.91 mW across the whole wafer.

undercut heater. The dark rectangular shade in the image indicates the underlying air cavity. (B) shows the SEM cross-section of an undercut heater cavity. One example heater tuning curve is shown in Fig. 14(C). The calculated power per π phase shift is 2.81 mW. This is 15 times lower than a non-undercut heater. Fig. 14(D) shows an example wafer map of power per π phase shift. We are able to achieve good uniformity across wafer, with variation limited to 2.7–2.9 mW.

X. Optical Testing

The manufacture of silicon photonic integrated circuits in high volumes requires process controls and product monitors similar to those implemented for conventional CMOS integrated circuits. In particular, most semiconductor manufacturers adhere to JECEC standards for wafer acceptance testing. This typically involves wafer-level inline test of scribe line test structures embedded between product die. None of the commercially available inline electrical test systems were found to be suitable for silicon photonics test so GLOBALFOUNDRIES developed a custom Inline Optical Test System (ILOTS) [19].

The ILOTS system enables wafer-level inline electro-optical test of photonic devices in an automated cost-efficient manner. It has been designed for high-throughput wafer acceptance testing but is flexible enough to enable detailed device characterization for process development. ILOTS consists of a custom photonic test head interfaced with a standard 300 mm wafer prober (TEL 8XL with auto loader). Vertical grating couplers and fiber optic cables bring C-, L-, or O-band optical signals to and from a wafer while a standard electrical probe card handles electrical signals. The tester aligns fibers to the gratings with an accuracy and repeatability better than ± 0.4 dB (σ). The test system is capable of characterizing optical, electro-optical, and opto-electric effects in our full suite of photonic devices. From this data we can extract photonic device parameters such as optical loss, cross talk, coupling length, V·pi·L, phase shift, optical responsivity, small-signal bandwidth, resonance frequencies, effective refractive index, group velocity, etc. A subset of these parameters are sampled on production wafers to monitor the process output and identify outlier wafers that are unsuitable for shipment.

Due to the variability in the coupled input light intensity most optical parameters of interest cannot be measured directly. Rather, we use a "cut-back" method to derive the underlying parameter from a series of related test structures. For example, to measure the silicon waveguide propagation loss we split the input light into multiple paths, each with a different length of waveguide, and measure the output of each path independently. A linear regression on the results eliminates losses due to the grating couplers and splitters and derive the average loss per length of waveguide. A similar approach is applied to most pure optical parameters while other methods are required for photodetector responsivity, phase shifter V·pi·L and some other parameters.

Fig. 15 depicts a typical test structure to measure insertion loss on a GLOBALFOUNDRIES ILOTS prober. Note that any excess bends and waveguides are 'balanced out' such that there are the same number of bends and length of excess waveguide in each branch (Fig. 16). This way the difference of the output signals directly carries the information about the insertion loss and absolute power measurements are not necessary. For wafer acceptance testing a sample of reticles on each wafer are measured in this fashion and the derived data are evaluated against an established specification limit as shown in Fig. 1.

XI. CMOS Devices

The integration of photonics into a CMOS technology offers a range of important new capabilities related to RF and digital circuits. Optical sub-assembly fabrication costs and power consumption can be substantially reduced in a monolithic RF CMOS technology by integrating complete transmitter (TOSA) and receiver (ROSA) optical paths on a single photonic integrated circuit (PIC). This may include monolithic implementation of the core transceiver electronics such as transmitter driver and receiver transimpedance amplifier (TIA), [20] limit amplifier and clock data recovery (CDR) functions alongside optical modulators, multiplexers, de-multiplexers, and detectors. CMOS integration can also extend to digital controller circuits (state machines) required for thermal stabilization or light source control in present on the chip but also high-speed serial links that are presently fabricated as a standalone application specific integrated circuit (ASIC).

The monolithic integration of CMOS electronics and photonic devices can bring important advantages in electro-optical performance and power consumption. Hybrid integration is burdened by significant parasitics at the interface between CMOS circuits and optical devices. These can be substantially reduced in a monolithic design; enabling higher bitrates and greater energy efficiency. The parasitic load between optical device and CMOS can be further reduced by avoiding ESD protection of transistor gates and optical devices when they are fabricated on a monolithic process. This is especially important for the receiver

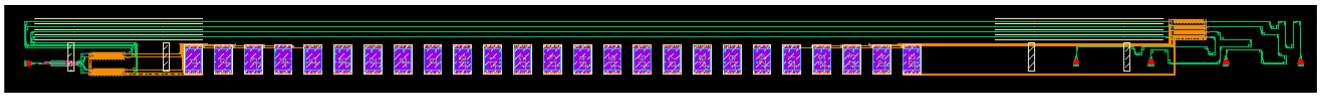


Fig. 15. Electro-optical pad cage with 1 input grating coupler on the left, a 1 × 4 way splitter, 1 × 25 electrical padset, and 4 output grating couplers. Also depicted are cleave streets for edge coupled measurements (US patent by IBM).

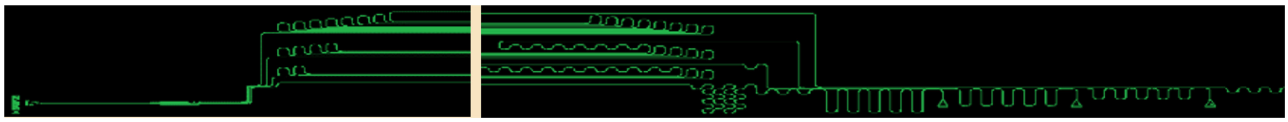
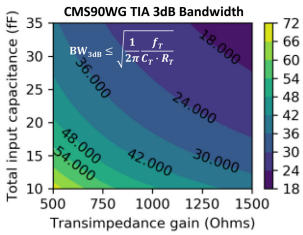


Fig. 16. Test structure for the measurement of SOI waveguide propagation loss. The excess bends and waveguides are balanced out (equalized) on each of the 4 optical paths. Only the delta between the outputs is relevant and directly proportional to length of the waveguide under test.



(a)

	14nmFF	22FDX	45CLO	CMS90WG
NMOS f_t	270GHz	350GHz	280GHz	150GHz
Supply Voltage	0.8V	0.8V	0.9V-1.1V	1.2V
Technology	BULK	SOI	SOI	SOI
Mx res and cap	high	low	very low	very low
Integration	hybrid	hybrid	monolithic	monolithic
-Parasitic load	*5-30fF	*5-30fF	2-3fF **	
-ESD diode	~50fF	~50fF	0	0
Expected TIA NRZ bitrate	50Gb/s [21]	>60Gb/s	100Gb/s	50Gb/s

* TSV: 5fF; uBump: 30fF ** metal interconnect

(b)

Fig. 17. (a) TIA 3 dB bandwidth as a function of input capacitance and transimpedance gain for the CMS90WG platform. (b) Expected performance characteristics of various GLOBALFOUNDRIES technology platforms.

circuitry where any parasitic capacitances at the input of the TIA may significantly limit the 3 dB bandwidth and total optical link modulation speed. Fig. 17(a) show an analytic relation of the 3 dB bandwidth of a TIA as a function of total input capacitance and transimpedance gain for the CMS90WG technology.

The monolithic integration of a photodetector and a TIA should be possible with total input capacitance (C_T) below 20–25 fF (including photodiode load, metal connection and the input stage load of a TIA) allowing to achieve high enough 3 dB TIA bandwidth to support 50 Gbaud per second. On the transmitter side, the monolithic integration will bring the most benefits when a compact, and low load optical modulator such a ring resonator or electro-absorption modulator (EAM) is used. In this case, due to the lack of interface parasitics (comparable to the device itself) the modulator driver can reach higher modulation speed or consume less power. Having integrated electronics next to photonic devices is also very useful for thermal tuning various optical devices. Due to temperature-induced dispersion effects in silicon, wavelength-division multiplexing (WDM) circuits typically require multiple tuning signals. For example, an eight-stage cascaded Mach-Zender demultiplexer requires accurate phase control of 11 delay lines. On-chip implementation through integrated digital circuits can dramatically reduce input/output pins. This is one area where a fully capable process design kit, one that supports simultaneous placement and simulation of optical and electrical devices, is important.

Coherent optical fiber communications present additional opportunities for integrated CMOS. First, to control transmitter optical circuits for phase-shift keying (PSK) and quadrature amplitude modulation (QAM). Second, to compensate for group-velocity dispersion (GVD) and polarization-mode dispersion (PMD) through digital signal processing in the receiver. These digital circuits must support high operating frequencies in order to keep up with the bitrates targeted for coherent applications.

The CMS90WG platform supports a full array of RF CMOS features. Dual gate dielectrics enable high-speed digital and analog FETs alongside 2.5 V input/output devices. These are supplemented with precision polysilicon resistors, an electrically programmable fuse (eFuse), electro-static discharge (ESD) protection diodes, and various capacitors and inductors. A seven-layer back-end-of-line (BEOL) stack enables complex on-chip interconnect while Cu wires and low-k dielectrics improve performance. The CMS90WG technology has an NFET Ft/Fmax of 148/224 GHz and should support TIA NRZ bitrates above 36 Gb/s in monolithic applications.

The next generation GLOBALFOUNDRIES silicon photonics platform, 45SPCLO, is under development and targets an improved CMOS NFET Ft/Fmax of 280/340 GHz. This platform will support monolithic drivers and TIA's operating above 50 Gbaud while offering additional advantages in circuit density, system power and packaging cost. Fig. 17(b), [21] compares several GLOBALFOUNDRIES CMOS technologies suitable for short-reach low-power photonics applications. Monolithic transceiver designs built on 45SPCLO are expected to support a TIA NRZ bitrate of 100 Gb/s.

XII. Process Design Kit

The CMS90WG technology is a monolithic photonic technology that allows designers to have optical and electrical circuits on the same IC. This technology is supported by a full process design kit (PDK) that includes scalable pcells and compact models that work within a Cadence environment. As with straight CMOS technologies, the models, including the photonic models, for CMS90WG employ nominal device parameters and tolerances that are based on in-line testing and wafers are subjected

to a published wafer acceptance criterion (WAC). Further, the models allow for optical and electrical co-simulation; so a full circuit simulation is possible within one tool. Lastly, EM field solver support is included for inductor and T-lines.

There are Calibre decks for DRC verification of layouts, for LVS comparison of schematics and physical layout, and for PEX. The ground rules include rules for all of the layers used in the photonic devices, as well as the electrical devices. In addition, the DRC checks that the waveguides are properly connected in terms of input/output ports, alignment, and dimension. There are scalable parametric cells for waveguides, directional couplers, and phase shifters; and there are fixed layouts for modulators, detectors, polarization splitter rotators, fiber couplers, and WDM MUX and DeMUX circuits. The modulators and WDM devices are hierarchical circuits built of standard kit elements and are modelled as such. Further, LVS recognizes these hierarchical cells and the ports associated with them.

To aid designers, there is also a waveguide path tool. This tool allows designers to trace a multi-segment path in layout. This path is then converted into various waveguide components (straight sections, tapers, and bends). In addition, a schematic view is generated for this path as well as a symbol view for that particular path.

The PDK is fully documented with a technology Design Manual containing technology definition, BEOL metal stack information, ground rules, and basic device information. There are Release Notes and User's Guides for the various tools and utilities, e.g., a DRC Release Notes and a ESD Reference Guide. Lastly, there is a Model Reference Guide that shows model-to-hardware correlation for both the electrical devices and the photonic devices

XIII. Reliability

As part of the foundry qualification for the CMS90WG technology, a comprehensive set of reliability stress evaluations were done across representative CMOS devices, photonic devices and back-end-of line (BEOL) wiring structures. The CMOS and BEOL stress plan was based on standard foundry CMOS technology standards, while the photonics stress plan was developed to evaluate the ability of the technology to support a Telecordia 468 standard qualification at a product level.

All CMOS and BEOL device stresses passed the requirements and behaved as expected based on experience from non-photonic 90 nm CMOS technology. An overview of the photonic device stress plan is shown in Table II. The photonic devices passed all stress requirements and provided the necessary data to set a maximum optical input power limit on the photodiode as a function of bias voltage.

TABLE II
Photonic Device Reliability Stress Plan

Stress	Stress Conditions
Photodiode – Electrical (Wafer)	Bias: 2.5 – 4.5V, T: 30, 85, 125, 150 C, Wi = 0.3, 0.5, 0.7, 0.9 um
Photodiode – Electrical (Module)	V =2.5, 85C and 3.0V, 175C, 2000 hr Wi = 0.5, 0.7, 0.9 um
Photodiode – Electo-Optical (Early)	Bias: float, 3.0, 3.5V, Optical power: 5, 11 dBm T: 25, 85 C, Wi = 0.5, 0.7, 0.9 um
Photodiode – Electo-Optical Power Step Stress	Bias: 1.5, 2.0, 2,5, 3.0, 3.5V Optical power: 0.5 to 9mW in 0.25mW steps T: 25 C, Wi = 0.7, 0.9 um
Photodiode – Electo-Optical	Bias: float, 1.32-3.0V, Optical power: 1-9 mW T: 25, 85 C, Wi = 0.7, 0.9 um
Junction Phaseshifter– Electrical (Wafer)	Bias: 6.5 – 8V, T: 30, 85, 125C,
Waveguide / Junction Phaseshifter	Thermal Cycle: -65 to 150 C, 1000 cyc
V-groove Proximity (Rings, WG, DGFET)	T&H (85C/85%), 500hr

XIV. Technology Development Roadmap

Technology development continues in effort to expand the base performance capability and device list offering of the CMS90WG silicon photonics technology in order to address higher performance market demands. Some examples of performance enhancements will include lower TE and TM loss fiber attach mode converters, high bandwidth modulators (>35 GHz) and high bandwidth photodetectors (>50 GHz). New device features planned to be added to the technology include low loss nitride waveguide, direct laser attach capability and avalanche photodetectors (APD).

The next-generation 45SPCLO photonics platform is under development and will feature significant performance improvement to the monolithic RF SOI CMOS (see details in Section XI) which will enable integrated monolithic drivers and TIA's operating at >50 Gbaud while also offering density, power and packaging cost advantages.

XV. Conclusion

A competitive 300 mm silicon photonics foundry technology (CMS90WG) has been developed and qualified by GLOBALFOUNDRIES for general availability which takes advantage of advanced 300 mm CMOS process technology and provides manufacturing scale. A state-of-art process design kit (PDK) offers a co-design environment with access to a comprehensive photonics device library along with a monolithically integrated SOI CMOS device library. The designer has the added flexibility to submit custom photonic device layouts to be used as-is or in conjunction with other standard devices. Advances in automated wafer level optical test enable statistical photonic device modeling and process control. Technology development investment continues to further improve the base performance and device list offering of CMS90WG and will extend to development of the next generation 45SPCLO platform.

Acknowledgment

The authors would like to thank Ted Letavic from GLOBALFOUNDRIES and Will Green from IBM for their technical leadership and guidance during the development and manufacturing qualification phases. Authors also thank the following team for their development engineering support: D. Riggs, A. Jacob, C. Meagher, Z. Sowinski, K. McLean, C. Hedges, P. Beliveau, B. Orner, B. Hedrick, A. Aboketaf, B. Harris, M. Nicewicz, and D. Sacher.

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