Hybrid 14nm FinFET - Silicon Photonics Technology for Low-Power Tb/s/mm^2 Optical I/O

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Abstract

We demonstrate a microbump flip-chip integrated 14nm-FinFET CMOS-Silicon Photonics (SiPh) technology platform enabling ultra-low power Optical I/O transceivers with 1.6Tb/s/mm^2 bandwidth density. The transmitter combines a differential FinFET driver with a Si ring modulator, enabling 40Gb/s NRZ optical modulation at 154fJ/bit dynamic power consumption in a 0.015mm^2 footprint. The receiver combines a FinFET trans-impedance amplifier (TIA) with a Ge photodiode, enabling 40Gb/s NRZ photodetection with -10.3dBm sensitivity at 75fJ/bit power consumption, in a 0.01mm^2 footprint. High-quality data transmission and reception is demonstrated in a loop-back experiment at 1330nm wavelength over standard single mode fiber (SMF) with 2dB link margin. Finally, a 4x40Gb/s, 0.1mm^2 wavelength-division multiplexing (WDM) transmitter with integrated thermal control is demonstrated, enabling Optical I/O scaling substantially beyond 100Gb/s per fiber.

Keywords: optical interconnect, silicon photonics, FinFET

Introduction

Exponentially growing demand for I/O bandwidth in datacenter switches and high-performance computing nodes drives the need for tight co-integration of optical interconnects with advanced CMOS logic, enabling high-density, power efficient and low-latency optical I/O for a wide range of interconnect distances (1m-500m+) [1]. Silicon photonics is a prime technology platform to realize the desired scaling in optical I/O cost and performance, by leveraging established CMOS manufacturing [2] and advanced 3-D integration methods. Here, we present a hybrid FinFET CMOS-SiPh technology realizing optical I/O transceiver density beyond 1Tb/s/mm^2, combined with record low dynamic power consumption of 230fJ/bit at 40Gb/s single-lane non-return-to-zero (NRZ) data rates. This is achieved through high-density, low-parasitic microbump flip-chip integration of compact, high-speed monolithic SiPh modulators and photodetectors, with co-designed highly power-efficient, high-speed circuits in bulk FinFET CMOS.

Technology Description

A. Silicon Photonics Chip

The SiPh chips (20mm^2) are manufactured on 300mm SOI wafers in an R&D CMOS fab [2]. They contain a dense 8-channel transmitter (TX) array and an 8-channel receiver (RX) array, both operating at 1330nm wavelength (Fig. 1). Each TX unit cell (0.015mm^2) contains a 7.5µm radius, 45fF, 30GHz Si ring modulator (RM) with integrated heater, whereas each RX unit cell (0.01mm^2) contains a 15x2µm^2, 30fF, 50GHz Ge waveguide photodetector (PD) with 0.9A/W responsivity. Fiber grating couplers are implemented on the north side of the chip for interfacing with a 12-channel, 250-µm pitch SMF V-groove array. Wirebond and RF probe pads are included for delivery of dc and high-speed signals respectively.

B. 14nm FinFET CMOS Chip

The 14nm FinFET chips (1.5mm^2) are manufactured in GlobalFoundries 14LPP technology, and mirror the design of the SiPh chip, having dense arrays of ultra-compact invertor-based modulator drivers and TIAs. The drivers are designed to produce a differential output swing of 1.6V_{DD}, maximizing the optical modulation amplitude (OMA) of the depletion-type ring modulator. The circuit architecture (270µm^2) is shown in Fig. 2. The design targets 40Gb/s NRZ data rate at the nominal 0.8V supply voltage, for a total capacitive load of 100fF. The TIA circuit architecture (<50µm^2) is shown in Fig. 2, and targets low-power operation with high sensitivity at 40Gb/s for a 120fF total input load, by balancing the transimpedance gain (1.6kΩ) and bandwidth (26GHz). A buffer amplifier is added to drive the electrical signal across a 50Ω on-chip transmission line into a high-speed RF probe for off-chip analysis on a high-speed sampling oscilloscope.

C. Flip-Chip Assembly and Packaging

The FinFET dies are flip-chipped onto known-good SiPh dies through microbumps with 50µm pitch and 30µm pad size, minimizing the interface parasitic capacitance to below 30fF. Next, the CMOS-SiPh assemblies are glued on test boards, wirebonded, and finally the SMF V-groove array is actively aligned and glued to the assembly (Fig. 1), achieving 4.5dB fiber-to-chip coupling losses.

Results

Fig. 3 shows the measurement setup used to test the transceiver. Fig. 4 illustrates single-lane TX performance: at nominal 0.8V supply and optimized RM heater tuning, 40Gb/s NRZ modulation is achieved with 4.2dB extinction ratio (ER) and 3.9dB insertion loss (IL), which is equivalent with a transmitter penalty TP=OMA/(2P_{IN}) of 9dB. The energy consumption (E_{bit}) is 154fJ/bit. Increasing the supply voltage to 0.9V enables modulation rates up to 52Gb/s. The RX performance, as measured with an external 44Gb/s $LiNbO_3$ modulator (ER>15dB), is summarized in Fig. 5. At 0.8V supply, and, wide open electrical eye diagrams with signal-to-noise (SNR) ratio above 9 are obtained at 40Gb/s data rate for average photocurrents as low as 42µA, equivalent with a waveguide-referred OMA sensitivity of -10.3dBm. The TX and RX are also tested in a loop-back configuration. In this experiment, 13dBm laser power is coupled into the SiPh chip, resulting in -4.2dBm fiber-coupled OMA at the TX output. The modulated light beam is subsequently attenuated off-chip by 2dB and coupled back into the RX. The resulting 32Gb/s electrical eye diagram recorded at the RX output (Fig. 6) is wide open with SNR>6. Finally, 4x40Gb/s WDM transmission is demonstrated from a cascaded SiPh RM array in Fig. 7. By appropriately tuning the integrated heater currents, the

operation wavelengths of the individual SiPh ring modulators can be tuned (11mW/nm) to the 2nm wavelength grid of a WDM laser source. Very uniform power efficiencies and OMA have been obtained for all tested channels. Finally, Table 1 summarizes the measured performance and compares with previous reports of CMOS-SiPh transceiver demonstrations. The presented results clearly stand out in terms of power efficiency, bandwidth density or both. Optimizations in SiPh device designs and CMOS circuit layouts are possible in future demonstrations, and are expected to further improve modulation rates and link margin.

Acknowledgements

This work has been supported by imec's industry-affiliation R&D program on Optical I/O.

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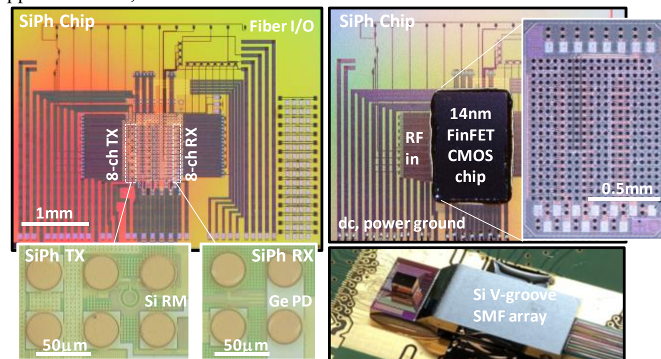


Fig. 1. SiPh and FinFET chip micrographs, including SiPh TX and RX unit cell details, and images of the fiber-packaged assembly.

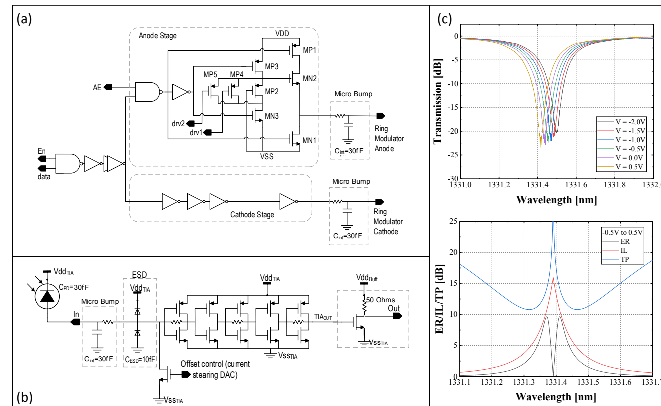


Fig. 2. (a) TX driver, and (b) RX TIA schematic. (c) SiPh RM: static optical transmission vs V_{bias} (top), and ER, IL, TP spectra for 1Vpp swing (bottom).

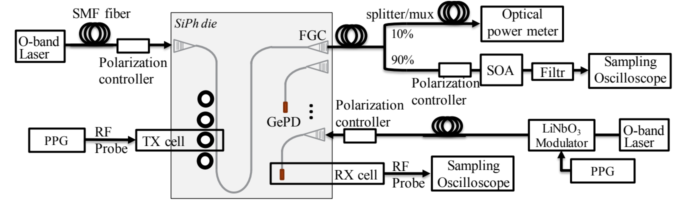
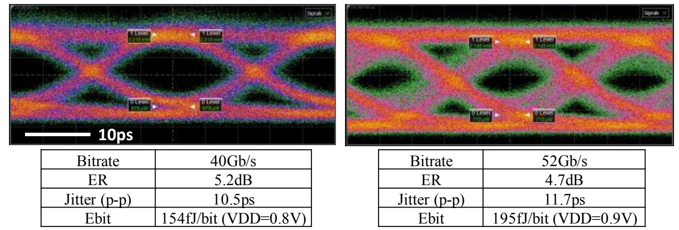


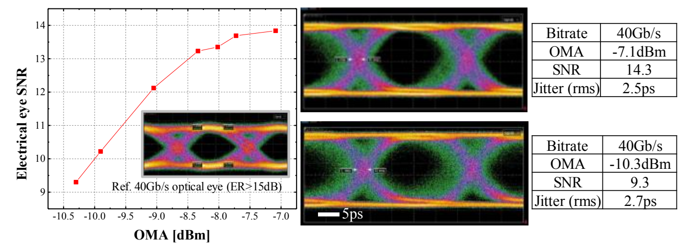
Fig. 3.Measurement setup schematic



Bitrate	40Gb/s
ER	5.2dB
Jitter (p-p)	10.5ps
Ebit	154fJ/bit (VDD=0.8V)

Bitrate	52Gb/s
ER	4.7dB
Jitter (p-p)	11.7ps
Ebit	195fJ/bit (VDD=0.9V)

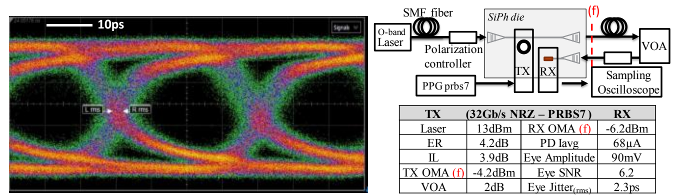
Fig. 4.TX eye diagrams: left 40Gb/s (PRBS31), right 52Gb/s (PRBS7).



Bitrate	40Gb/s
OMA	-7.1dBm
SNR	14.3
Jitter (rms)	2.5ps

Bitrate	40Gb/s
OMA	-10.3dBm
SNR	9.3
Jitter (rms)	2.7ps

Fig. 5. RX at 40Gb/s (PRBS31). Left: Electrical eye diagram SNR vs. OMA Right: eye diagrams at OMA = -7.1dBm and OMA = -10.3dBm.



TX	(32Gb/s NRZ – PRBS7)		RX
Laser	13dBm	RX OMA (f)	-6.2dBm
ER	4.2dB	PD Iavg	68µA
IL	3.9dB	Eye Amplitude	90mV
TX OMA (f)	-4.2dBm	Eye SNR	6.2
VOA	2dB	Eye Jitter(rms)	2.3ps

Fig. 6. TX-to-RX loop-back performance at 32Gb/s.

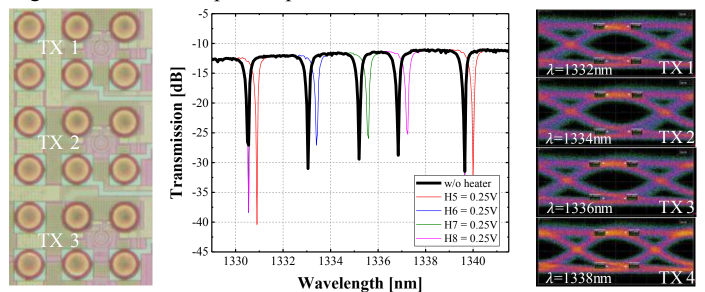


Fig. 7. WDM TX. Left: chip micrograph. Middle: static TX optical transmission. Right: 4λ x 40Gb/s eye diagrams (PRBS31).

TABLE I. Performance overview and benchmarking

	This work	**[3]**	**[4]**	**[5]**	**[6]**	**[7]**
Year of Publication	2018	2015	2015	2015	2012	2012
Integration Method	50um pitch Cu Flip Chip	Monolithic	Wafer-to-Wafer Through-oxide Via	150um pitch C4 Flip Chip	25um pitch microsolder Flip Chip	Monolithic
Technology (CMOS)	14nm LPP bulk FinFET CMOS	45nm CMOS SOI "zero change"	65nm CMOS bulk	40nm LP CMOS	40nm CMOS	130nm CMOS SOI
Technology (Si Photonics)	28nm SOI		65nm SOI	130nm SOI	130nm SOI	
I/O Bandwidth Density	**1.6Tb/s/mm²**	400Gb/s/mm²	500Gb/s/mm²	90Gb/s/mm²	1.6Tb/s/mm²	12.5Gb/s/mm²
Wavelength	1330nm	1183nm	1529nm	1550nm	1550nm	1560nm
Supply Voltage	0.8V	1V	1.2V	1.3V	1V,1.3V,2V	1.2V/-1.2V
Single-Lane Data Rate	**40Gb/s NRZ**	5Gb/s NRZ	5Gb/s	20Gb/s NRZ	10Gb/s NRZ	25Gb/s NRZ
TX (Ring Modulator)						
Driver Power	**154fJ/bit**	30fJ/bit	10fJ/bit	1.3pJ/bit	135fJ/bit	8.3pJ/bit
ER	4.2dB	6.5dB	5dB	>7dB	7dB	6.9dB
IL	3.9dB	4dB	1dB	n/a	n/a	n/a
#WDM channels	4	1-11	1	4	8	n/a
Ring Tuning Power	11mW/nm	2.5mW	n/a	6.2mW/nm	5.3mA/nm	n/a
Bandwidth per fiber	**160Gb/s**	5-55Gb/s	5Gb/s	80Gb/s	80Gb/s	25Gb/s
RX (Ge WPD)						
TIA power	**75fJ/bit**	~400fJ/bit	240fJ/bit	580fJ/bit	120fJ/bit	1.92pJ/bit
Rx sensitivity	-10.3dBm OMA	-5dBm OMA	-16dBm OMA	-7.2dBm Pavg	-15dBm Pavg	-6dBm Pavg